MP MASTER
MA29322

Wandel & Goltermann
Electronic Measurement Technology

UTI-1
BN 9537/01

Description and Operating Manual

Book 1

Order Number:
BN 9537/00.82

Wandel & Goltermann Tech., Inc.
1030 Swabia Court
P.O. Box 13585
Research Triangle Park,
North Carolina 27709-3585

Phone No: (919) 941-5730
Tlx No: 810-621-0002
FAX No: (919) 941-5751

23 July 91/.025/WGT

UTI-1 Introduction and General Information 1

UTI-1 Mainframe Specifications 2

UTI-1 Mainframe Operating Description 3

UTI-1 Module Design Guidelines 4

Interchangeable Test Adapter Design Guidelines 5

IEEE-488 Bus Interface, BN 9537/00.01 6

Digital Interface, BN 9537/00.02 7

Analog Interface, BN 9537/00.03 8

6 × 8 Switching Matrix, BN 9537/00.04 9

Custom Termination Module, BN 9537/00.06 10

Digitized by the Internet Archive
in 2025

https://archive.org/details/manualsplus_06343

1. UTI-1 Introduction and General Information

Contents

		Page
1.1.	Introduction	1.1-1
1.1.1	Reducing costs with the UTI-1	1.1-1
1.1.2	Special features	1.1-1
1.2.	UTI-1 General Information	1.2-1
1.2.1	Safety precautions	1.2-1
1.2.2	Ventilation and rack mounting	1.2-2
1.2.3	Power supply and fuses	1.2-3
1.2.4	Powering up the UTI-1	1.2-4

1.1. Introduction

1.1.1 Reducing costs with the UTI-1

In automatic testing, the interface between the Unit Under Test (UUT) and the Automatic Test Equipment (ATE) plays a major role. Unfortunately, custom interface design is frequently necessary due to the demanding bandwidth, power, signal routing, and noise level requirements. Custom design is time consuming and costly, both initially and during the life of the system because of the difficulty of obtaining proper documentation, special components and system specialists.

However, there is a simple solution: the UTI-1 Universal Test Interface from Wandel & Goltermann. Flexible through its modular design, it offers an economically viable alternative to custom interface design.

1.1.2 Special features

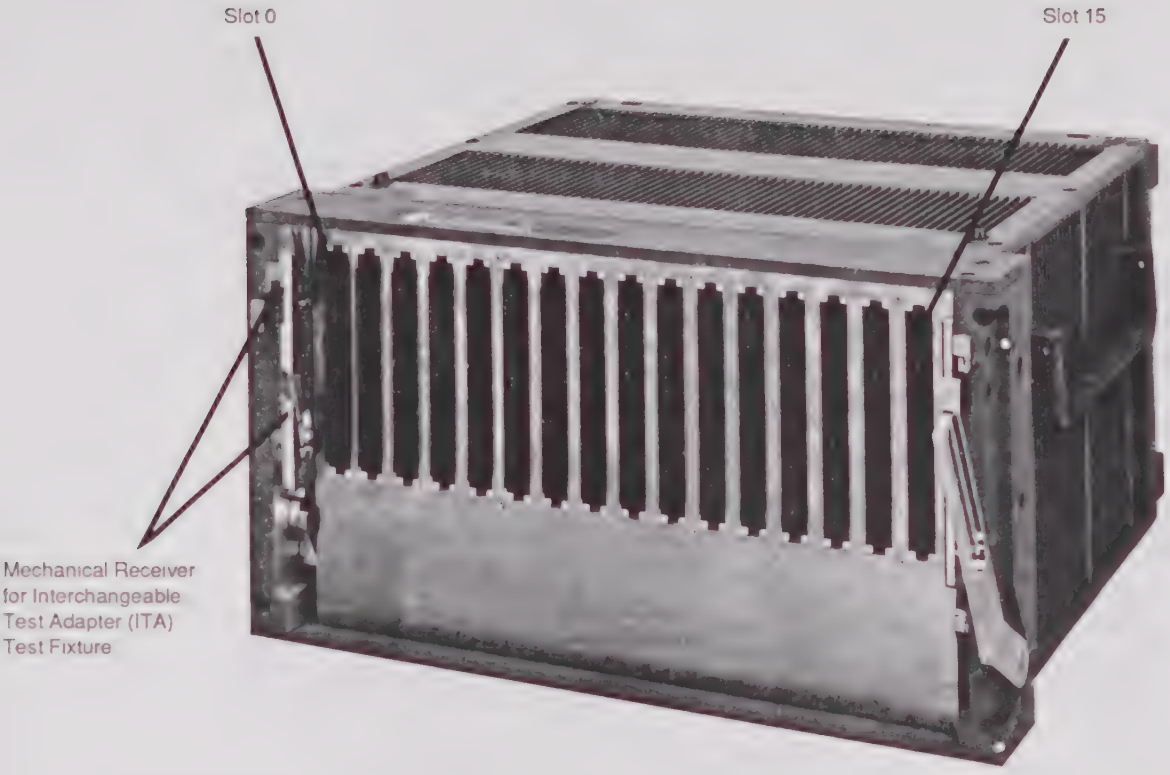
Simple Test Fixture Solution

The UTI-1 interfaces custom or turn-key ATE systems by combining ATE interfacing, direct test fixture mounting, and signal routing and switching capabilities all in one rack mountable unit. These functions are implemented using a three-sided access environment:

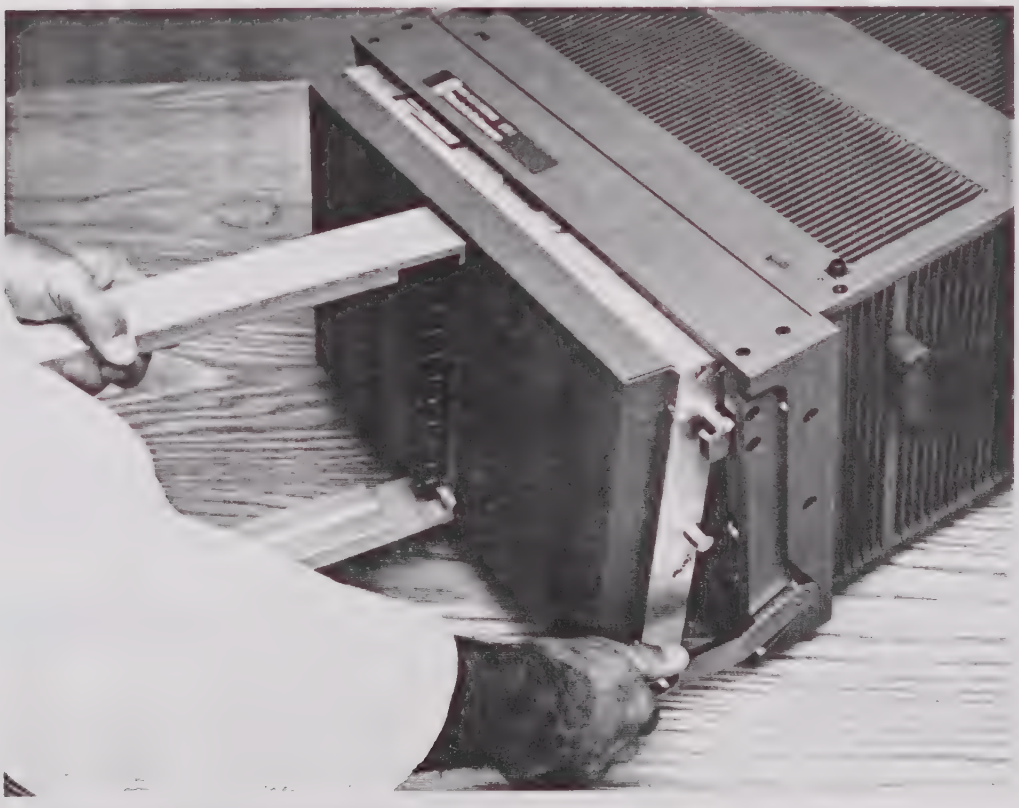
1. A large horizontal mother board provides signal routing between the modules and the control bus. The bottom side of the interface modules interconnect to the mother board via ZIF lock connectors.
2. External instruments can interface to the rear of some individual modules.
3. Direct electrical/mechanical connection to the UUT is possible at the front connector of the module.

Modularity and Flexibility

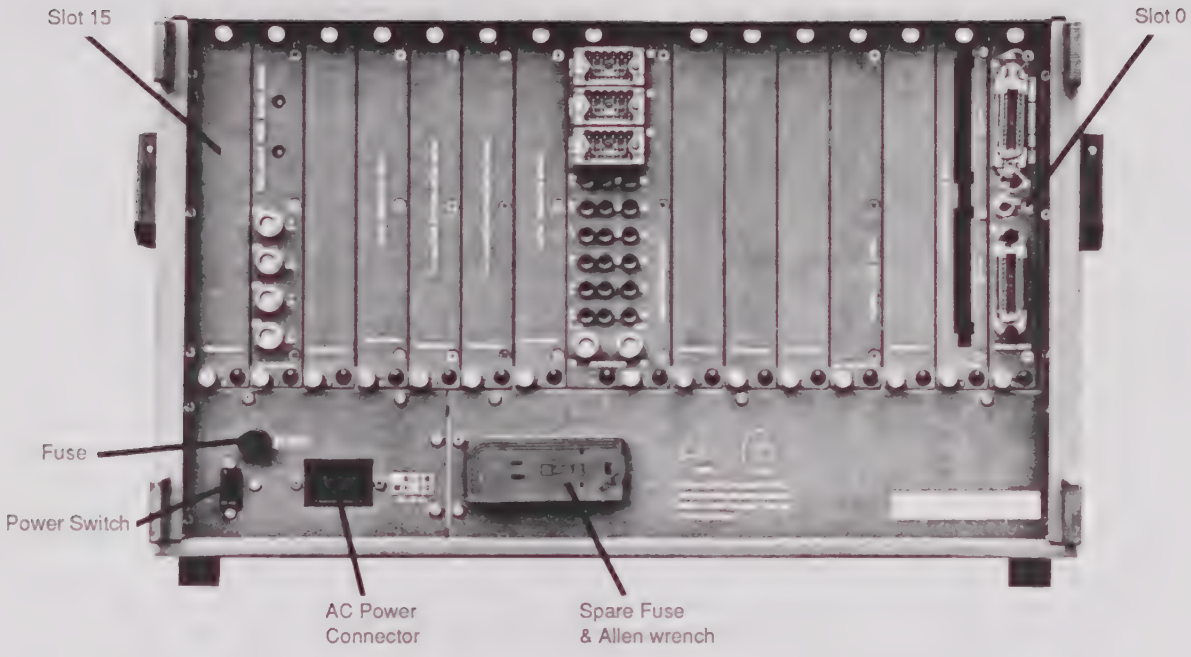
The modular and flexible construction of the UTI-1 permits easy reconfiguration of the test set-up when implementing tests on a newly developed UUT. The UTI-1 can adapt to your future product developments, and thereby significantly reduce your interfacing costs. With its family of off-the-shelf interface modules providing easy and economical reconfiguration, the UTI-1 also allows connection of general purpose test instruments to your test objects.



Front view of the UTI-1 with mechanical receiver for the Interchangeable Test Adapter (ITA) Test Fixture.



Changeover of the ITA/Test Fixture is quick and easy; just pull the handle down, replace the fixture and push the handle back up.



Rear of the Universal Test Interface (UTI-1) with the interface modules and blank panels installed.

Rear view of the UTI-1 while using the Allen Key to open or close the ZIF Lock connector for installation or removal of the UTI-1 Interface Modules.

1.2. UTI-1 General Information

1.2.1 Safety precautions

A.C. line voltage

Before switching on the equipment, make sure that it is set for the correct line voltage. This voltage is preset at the factory and indicated on the rear panel with a silver dot.

Safety Class

This is a safety Class I instrument (see IEC 348 or VDE 0411.) To ensure compliance with safety regulations, the A.C. line plug must be connected to an A.C. socket having a protective ground connection. Do not allow this connection to be interrupted or disconnected inside or outside of the apparatus. Failure to heed this warning can make the apparatus dangerous to operate.

Protective ground connection

Before beginning any measurements with the instrument, ensure that a protective ground connection has been made. If the protective ground conductor of the A.C. line is suitable, then plug the instrument into the A.C. line first. Then connect the ground conductor of the measuring circuit to the instrument casing before connecting the rest of the test circuit.

Safety procedure for damaged or malfunctioning instruments

If the instrument:

- shows visible damage,
- fails to perform the intended measurements,
- or has possibly been damaged,

then it should be considered hazardous. Turn off the power, disconnect the instrument, and secure it to prevent further operation until it has been repaired.

Fuses

Use only the specified fuses.

Opening the instrument

At some point it may be necessary to remove the instrument covers to carry out repairs, maintenance, and adjustments. Since this can expose live circuits, disconnect the instrument from all power sources before opening it. Repair, maintenance, and calibration of the equipment should not be carried out by anyone other than trained technicians who are aware of the hazards involved.

Repairs

Trained technicians should handle all repairs, while avoiding any alterations to the safety features of the instrument. In particular, do not modify clearance allowances or insulation characteristics.

Spare parts

Use only specified spare parts, as the use of other parts can make the instrument unsafe.

Safety tests after repair and maintenance

Protective ground conductor test

Check the cable for visible signs of damage and poor connections. Measure the resistance of the protective ground conductor between the A.C. plug contact and the instrument casing. The resistance should be less than 0.5Ω. Shake the cable during the measurement: variations in resistance mean that the cable is faulty.

Insulation test

Measure the insulation resistance between the A.C. line conductor terminals (shorted together) and the protective ground terminal of the instrument using a 500V D.C. insulation tester. (The A.C. line switch of the instrument must be in the "ON" position.) The insulation resistance must be greater than 2 MΩ.

1.2.2 Ventilation and rack mounting

Temperature and ventilation

The UTI-1 was designed for an ambient temperature range of +5°C to +40°C (41°F and 104 °F.) Since the instrument does not employ forced ventilation, do not obstruct the convectional air flow through the instrument by covering the ventilation slots in the panels. When stacking several instruments together, ensure that the upper temperature limit will not be exceeded.

Rack mounting

Since the case dimensions conform to DIN 41 494, IEC 297 and ASA C 83.9 (USA), the instrument fits into a 19" rack.

For rack mounting, remove the instrument feet, plastic guides, and folding carrying handles. See figure 1.2.

Temperature within the rack

With rack mounting ensure that the maximum temperature limit is not exceeded. Leave a space of 1 U (44.4 mm or approximately 1.75") above and below the instrument. However, you may cover the spaces at the front of the rack with dummy panels.

Ventilation

Ensure that adequate rack ventilation is provided. If a fan is used, it should draw air through a filter in order to minimize dust accumulation problems.

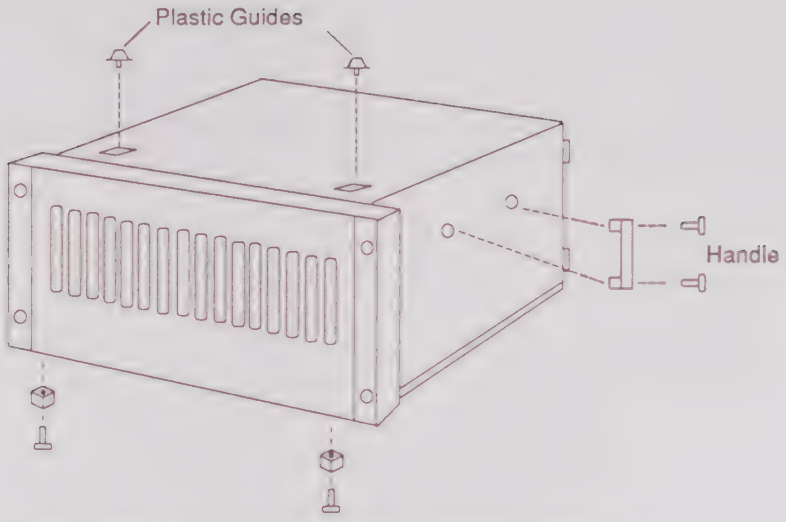


Figure 1.2 Converting the bench model for rack mounting.

1.2.3 Power supply and fuses

A.C. line frequency

The UTI-1 can operate with an A.C. line frequency between 47 and 63 Hz. The nominal line voltage range is either 95V to 130V or 192V to 258V.

Setting the A.C. line voltage

Set the A.C. line voltage to 120V or 220V by changing the power supply jumper. To locate this jumper, remove the bottom cover of the UTI-1 and the power supply cover. The jumper is clearly marked on the power supply circuit board.

Fuses

We specify the following fuse values and types:

Series A-C:
120V: 2 amp fast
220V: 1 amp fast
Series D...
120V: 5 amp normal
220V: 5 amp normal

A.C. line connection

In accordance with the specifications of VDE 0411 or IEC 348 Safety Class I, the instrument casing is directly connected to the protective ground conductor. For this reason, the following rules are important:

1. Only connect the instrument to an A.C. socket having a protective ground contact.
2. Use the A.C. line cable supplied with the instrument whenever possible. If you use another cable, it must have a protective ground conductor.

1.2.4 Powering up the UTI-1

A. C. line switch

The A. C. line switch is located in the lower right-hand rear corner of the UTI-1. In the "ON" position, the button color changes to red.

2. UTI-1 Specifications

Contents **Page**

2.1. Motherboard Specifications 2.1-1

2.2. Power Supply Specifications 2.2-1

2.3. General Specifications 2.3-1

2.4. Ordering Information 2.4-1

2.4.1 UTI-1 Universal Test Interface 2.4-1

2.4.2 Optional Modules 2.4-1

2.4.3 Accessories 2.4-1

2.1. Motherboard Specifications

Signal Bus Specifications

Unbalanced Signal Lines 50
- Maximum Insertion Loss @ 1 MHz(Slot 1 to 15) (75Ω termination) . . . . . ≤0.1dB
- Frequency Range . . . . . DC to 20 MHz
- Frequency Response (referenced to 1 MHz) (75Ω termination) . . . . . ≤0.6dB
- Crosstalk (75Ω termination) . . . . . >65 dB @ 1 MHz*
  . . . . . >40 dB @ 20 MHz*
- Capacitance
  - Line to line . . . . . ≤130 pf
  - Line to chassis ground . . . . . ≤130 pf

Daisy Chained Lines (Series D... only) 17
- Insertion Loss @ 1 MHz (75Ω termination) . . . . . ≤0.02 dB
- Frequency Range . . . . . DC to 20 MHz
- Frequency Response (referenced to 1 kHz) (75Ω termination) . . . . . ≤0.05 dB
- Crosstalk (75Ω termination) . . . . . >65 dB @ 1 MHz*
  . . . . . >45 dB @ 20 MHz*
- Capacitance
  - Line to line . . . . . ≤20 pf
  - Line to chassis ground . . . . . ≤10 pf

Balanced Signal Lines 8

Maximum Insertion Loss (Slot 1 to 15) @ 1 kHz (600Ω termination) . . . . . ≤0.05 dB
- Frequency Range . . . . . DC to 620 kHz
- Crosstalk (600Ω termination) . . . . . >70 dB @ 620 kHz*
  . . . . . >114 dB @ 5 kHz*

Capacitance
- Tip to Ring . . . . . ≤130 pf
- Line to line . . . . . ≤130 pf
- Line to Chassis . . . . . ≤130 pf

Auxiliary Power Supply Bus Pairs 5
- Maximum Voltage . . . . . 150 volts
- Maximum Power Load . . . . . 150 V @ 800 mA
  . . . . . 15 V @ 8 A

Programmable Power Supply Bus Pairs 8
- Maximum Voltage . . . . . 150 volts
- Maximum Power Load . . . . . 150 V @ 400 mA
  . . . . . 15 V @ 4 A

*** Worst case value. More favorable bus combinations considerably improve crosstalk specifications.**

2.2. Power Supply Specifications

Series A through C

+5V Output
- Adjustment Range . . . . . .+.25V,-.1V
- Output Current . . . . . 1 to 11 Amp

+15V Output
- Adjustment Range . . . . . .none
- Output Current . . . . . 0 to 1 Amp
- Voltage Accuracy . . . . . ±5%

-15V Output
- Adjustment Range . . . . . .none
- Output Current . . . . . 0 to 1 Amp
- Voltage Accuracy . . . . . ±5%

Ripple
- +5V . . . . . <20 mV p-p at 20 MHz bandwidth
- ±15V . . . . . ≤5V p-p at 20 MHz bandwidth

Output Power
- Maximum combined output power . . . . . .75 Watts

All of the outputs are protected against short circuit and over voltage. The power supply ripple appears mainly at power line frequency and its first harmonic.

Series D...

+5V Output
- Adjustment Range . . . . . ±0.25V
- Output Current . . . . . 0 to 15 Amp

+15V Output
- Adjustment Range . . . . . ±0.75V
- Output Current . . . . . 0 to 4 Amp

-15V Output
- Adjustment Range . . . . . ±0.75V
- Output Current . . . . . 0 to 4 Amp

Ripple
- +5V, ±15V . . . . . <25 mV p-p at 20 MHz bandwidth

Output Power
- Maximum combined output power . . . . . 175 Watts

All of the outputs are protected against short circuit and over voltage. The power supply ripple appears mainly at power line frequency and its first harmonic.

Series E ...

+5V Output
- Adjustment Range . . . . . ±0.25V
- Output Current . . . . . 0 to 25 Amp

+15V Output
- Adjustment Range . . . . . ±0.75V
- Output Current . . . . . 0 to 4 Amp

-15V Output
- Adjustment Range . . . . . ±0.75V
- Output Current . . . . . 0 to 4 Amp

Ripple
- +5V, +15V . . . . . <25mV p-p at 20 MHz bandwidth

Output Power
- Maximum Combined Output Power . . . . . 175 Watts

All of the outputs are protected against short circuit and over voltage. The power supply ripple appears mainly at power line frequency and its first harmonic.

2.3. General Specifications

Power Supply
Nominal ranges of use of A.C. line voltage
selectable 95-130V/192-258V
Nominal range of use of A.C. line frequency
. . . . . 47 to 63 Hz
Safety class to IEC 348 and VDE 0411
. . . . . .Class I

Ambient Temperature Range
Nominal range of use . . . . . +5° C to +40° C
Storage and transportation . . . . . -20° C to +60° C

Dimensions (w × h × d in mm)
Bench and 19" Rack mounting model
. . . . . .482 × 267 × 482 (19" × 10.5" × 19")
Weight . . . . . approx. 21.5 kg (47.5 lbs.)

2.4. Ordering Information

2.4.1 UTI-1 Universal Test Interface

UTI-1 Universal Test Interface . . . . . BN 9537/01

2.4.2 Optional Modules

IEEE-488 Bus Interface . . . . . BN 9537/00.01
Digital Interface . . . . . BN 9537/00.02
Analog Interface . . . . . BN 9537/00.03
6 × 8 Balanced Switching Matrix . . . . . BN 9537/00.04
Custom Termination . . . . . BN 9537/00.06
2 × 32 Balanced Switching Matrix . . . . . BN 9537/00.23
Standard Latch Module . . . . . BN 9537/00.24
Oscilloscope Probe Access Module . . . . . BN 9537/00.25
Parallel Bus Interface . . . . . BN 9537/00.27
Parallel Bus Extender . . . . . BN 9522/00.01

– Subject to change without notice –

2.4.3 Accessories

Front and Back Panel for empty card slot (1 set) . . . . . BN 9537/00.08

UTI-1 Accessory Kit . . . . . BN 9537/00.26

This includes:

1	ITA Frame
10	64 Pin Connector Shell
10	Hardware for mounting Connector Shell
300	Pins (wire-wrap)

The above Accessory Kit is available to configure a custom Interchangeable Test Adapter (ITA) for your test head requirements.

– Subject to change without notice –

3. UTI-1 Mainframe Operating Description

Contents **Page**

3.1. Detailed Description of Features 3.1-1
3.1.1 UTI-1 Printed Circuit Boards 3.1-1
3.1.2 UTI-1 Motherboard Connections 3.1-1
3.1.3 Daisy Chained Lines 3.1-2

3.2. Four Bit Parallel Bus (Motherboard Connections) 3.2-1
3.2.1 General Hardware Description 3.2-1
3.2.2 Four Bit Parallel Bus Line Descriptions 3.2-1
3.2.3 Programming Word 3.2-2
3.2.3.1 Programming Words to Write to a UTI-1 Module 3.2-2
3.2.3.2 Programming Words to Read Data from a UTI-1 Module . . .3.2-4

3.3. Four Bit Parallel Bus Control Expansion Connection 3.3-1
3.3.1 General Hardware Description 3.3-1
3.3.2 Four Bit Parallel Bus Lines Description 3.3-2
3.3.3 Programming Word 3.3-5
3.3.3.1 Writing to Buffer Stores 3.3-6
3.3.3.2 Reading from Buffer Stores 3.3-9

3.3.4 Sample Buffer Store 3.3-11
3.3.4.1 Four Bit Parallel Bus Connection 3.3-12
3.3.4.2 Parallel BCD Instrument Connection 3.3-13

3.4. Sixteen Bit Parallel Bus 3.4-1
3.4.1 General Description 3.4-1
3.4.2 16 Bit Parallel Bus Line Descriptions 3.4-1
3.4.3 16 Bit Parallel Bus Operation 3.4-2
3.4.3.1 Overview of Read/Write Operation 3.4-3
3.4.3.2 Bus Time Outs 3.4-4
3.4.3.3 Address Range Assignment 3.4-5

3.4.4 Absolute Addresses 3.4-6
3.4.5 Standard UTI-1 Module Registers 3.4-6

3.5. Support Information 3.5-1
3.5.1 Circuit Description 3.5-1
3.5.1.1 Power supply 3.5-1
3.5.1.2 Fan Circuits 3.5-1

3.5.2 Schematic Diagram / Parts List 3.5-3

3. UTI-1 Mainframe Operating Description

3.1. Detailed Description of Features

3.1.1 UTI-1 Printed Circuit Boards

UTI-1 pc boards have three mating planes:

* Two 100-pin edge connectors along the bottom edge to mate with the UTI-1 motherboard.
* A 64-pin connector on the front edge to mate with the personality board on the ITA.
* Various rear panel connectors for interfacing to an external test system.

Each slot on the motherboard has two lever-actuated, 100-pin connectors to grab or release the card. Turning the lever to the release position simultaneously breaks all 200 connections between the motherboard and the pc board. Once released, the module can be easily exchanged after loosening two thumb screws on the module rear panel.

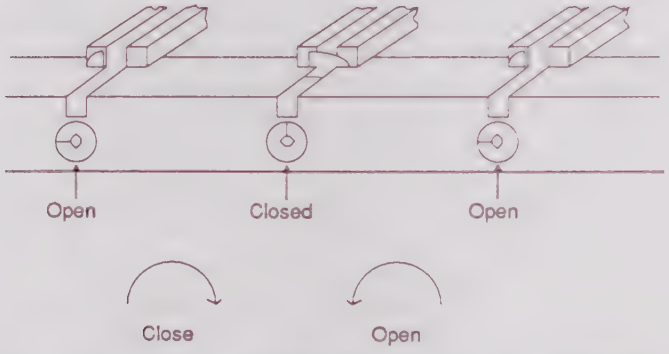


Figure 3.1.1 Module Release Mechanism (ZIF Connector)

3.1.2 UTI-1 Motherboard Connections

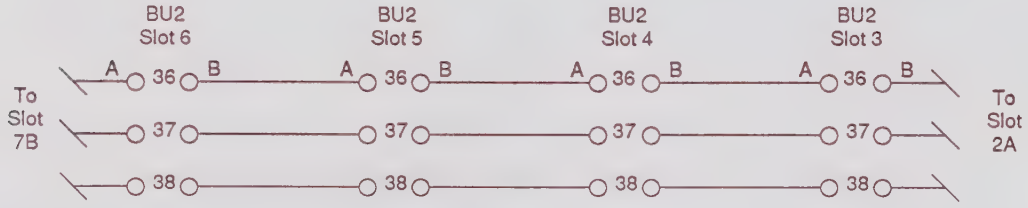
The UTI-1 motherboard consists of 16 slots, and each slot contains two 100-pin connectors designated as Bu1 and Bu2. Section 3.4.3 contains the signal names. The motherboard connections to all pins of slots 1 through 15 are the same. Since slot 0 is used only for the computer interface card, it has special motherboard connections.

The following is a general description of the basic types of motherboard lines:

45 lines:	Dedicated lines from the controller card in slot 0 to the other 15 slots. There are 15 card select lines and various four/sixteen bit parallel bus lines.
17 lines:	Daisy Chained lines between each pair of adjacent slots from slot 1 to slot 15. These lines are available in Series D... only.
74 lines:	Signal and voltage lines running from slot 1 to slot 15.
45 lines:	Ground, 5 volts, 15 volts, and -15 volts from the UTI-1 power supply.

3.1.3 Daisy Chained Lines

Daisy chained lines 0 through 16 connect between adjacent pairs of cards in slots 1 through 15. Each "A" pin is connected to the "B" pin on the adjacent slot. This arrangement allows signals to be used by a limited number of cards, and the same lines can be used for other signals between different cards.



Note: The Daisy Chained Lines are available in UTI-1 series D... .

Figure 3.1.3 Daisy Chained Bus Wiring Example

3.2. Four Bit Parallel Bus (Motherboard Connections)

The Four Bit Parallel Bus is one of the two busses permitting communication between the system controller and the UTI-1 modules. There is also a high speed 16 Bit Parallel Bus. Of the two available computer interfaces, the IEEE Interface module supports only the Four Bit Parallel Bus, while the Parallel Bus Interface module supports both the Four Bit Parallel Bus and the 16 Bit Parallel Bus.

3.2.1 General Hardware Description

To provide testing flexibility, UTI-1 modules have controllable elements such as relays, logic circuits and microprocessors. The system controller, together with the operating program, transmits control data to these elements. A program output statement addresses and changes the state of the appropriate elements. In addition, information can be passed from the UTI-1 modules to the system controller for analysis by the program. The Four Bit parallel bus hardware, contained in the IEEE Interface module or the Parallel Bus Interface module, provides the link between the UTI-1 and the system controller.

Data is transmitted in both directions between the system controller and the UTI-1 modules. The IEEE Interface module or the Parallel Bus Interface module, located in slot 0 of the UTI-1, converts the format. The data is transmitted from the controller to the UTI-1 where it is reformatted and sent in bit parallel, byte serial form to a particular UTI-1 module. The data is then latched by parallel latches. These latches are loaded one by one and the data is made available to the controllable elements of the UTI-1 modules.

Data can also be transmitted from the UTI-1 modules to the controller. Data transfer on the 4 Bit Parallel Bus is also in bit parallel (4 bits), byte serial form.

3.2.2 Four Bit Parallel Bus Line Descriptions

The computer interface module in slot 0 provides the signal lines on the Four Bit Parallel Bus with program data and commands. These lines are as follows:

* The $\overline{T}$/L ($\overline{Talk}$/Listen) line connects the computer interface module in slot 0 to the other 15 slots via the UTI-1 motherboard. The state of this single line indicates the direction of data flow. Low indicates talk and high indicates listen.
* The 15 card select lines ($\overline{CS1}$ to $\overline{CS15}$) connect the computer interface module in slot 0 to one of the other slots (slot 1 through 15) via the UTI-1 motherboard. A low pulse is sent to a particular module for each data position being written. The data in the "A" position of the program word controls these select lines. See the Description of the Program Word for further information.
* Four position lines (POS 2^0, POS 2^1, POS 2^2, POS 2^3), together with the card select lines, address the element needed for communication with the system controller. While the card select lines select a particular module, the data position lines select one of sixteen possible latches (each latch is 4 bit binary) within the selected module. The logic of these lines is positive true.

* Four talk lines (TALK 2^0, TALK 2^1, TALK 2^2, TALK 2^3) provide the data to the controlled element. The range of binary data is the ASCII characters 0 through 9, : , ; , < , = , > , and ?. They are equivalent to decimal values 0 through 9, 10, 11, 12, 13, 14, and 15 respectively, if the four leftmost digits are stripped off the 8 bit character. For proper Four Bit Parallel Bus operation, the computer interface module in slot 0 removes the four leftmost bits of each character sent by the computer, leaving the four rightmost digits for evaluation. The logic of these lines is positive true.
* Four listen lines (LISTEN 2^0, LISTEN 2^1, LISTEN 2^2, LISTEN 2^3) are used to send data back to the system controller. The range of binary data is 0 through 15. Data above 9 will be converted in the computer interface simulator to the ASCII characters :, ; , < , = , > , and ?. Prior to transmission to the controller, the four leftmost bits are added to reflect these characters. The logic of these lines is positive true.

3.2.3 Programming Word

There are two forms of the programming word: one for sending (writing) information to a UTI-1 module from the system controller, and the other for reading (interrogating) information from the UTI-1 module. The programming word is sent as a string by the program. These words are comprised of the "W" and "I" blocks and have defined structures. Each position or group of positions within the structure has a definite meaning.

The first string character ("W" or "I") in the programming word controls the direction of data travel. One programming word string may specify one or more data transfers (all in the same direction) by specifying a range of addresses. The data transfers proceed sequentially starting with the first address specified in the string.

3.2.3.1 Program Words to Write to a UTI-1 Module

The word has the following format:

"W X S_1 S_2 a b c d e f g h i j k l m n o p"

Where:

W: Word identifier "W" identifies the string as a write command.

X: Auxiliary equipment address: an address used internally by the computer interface module in slot 0 to differentiate between the 4 Bit Parallel Bus on the motherboard and the Buffer Stores (parallel latches) connected to the external 4 Bit Parallel Bus connector (Bu 2). The auxiliary equipment address of the UTI-1 motherboard bus is "1".

S_1: Starting Position Selector specifies the first address in the data transfer. It must be in the range A to P.

S_2: Ending Position Selector. This specifies the last address in the data transfer. It must be in the range A to P and equal to or greater than S_1.

a-p: The actual data to be transferred over the four talk lines. Since there are 16 possible values, each position is coded as one of the 16 consecutive ASCII characters starting with "0" (0123456789:;<=>?). The first character corresponds to the data sent to the address specified in S_1. Each additional character determines the data sent to each successive address until S_2 is reached. The number of data characters must match the range of data positions specified by S_1 and S_2.

Note: If S_1 is "A", the first character is decoded as a card select. The data in this position selects a particular UTI-1 module containing the elements to be controlled. The hardware on the UTI-1 modules must be designed to ignore the "A" position selection.

Example:

"W1AC59?"

W: Selects the data transfer direction for the UTI-1 module.

1: Auxiliary equipment address.

A: The first element addressed is A.

C: The last element addressed is C.

5: Element A receives the binary equivalent of ASCII 5 or 0101, corresponding to the state of the four Talk lines. The data that follows will be written to the module in slot 5. This card select information is latched in the computer interface and will not change unless a program word is sent that writes a different value in the "A" position. For example, if the next programing word sent is "W1BC12", the information in positions "B" and "C" will be again sent to the module in slot 5.

9: Element B receives the binary equivalent of ASCII 9 or 1001.

?: Element C receives the binary equivalent of ASCII ? or 1111.

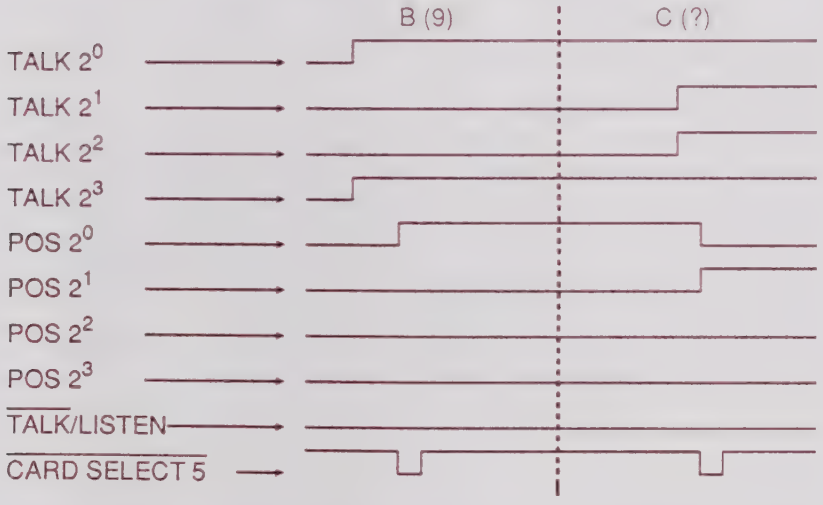


Figure 3.2.3.1 Transmission sequence on the 4 Bit Parallel Bus in the Talk Mode.

3.2.3.2 Programming Words to Read Data from a UTI-1 Module

The programming word has the following format

"I X S_1 S_2"

Where:

I: Identifies the string as a read command.

X: Auxiliary equipment address: an address that is used only by the computer interface module in slot 0 to differentiate between the 4 Bit Parallel Bus on the motherboard and the Buffer Stores (parallel latches connected to the external 4 Bit Parallel Bus connector). The auxiliary equipment address of the UTI-1 motherboard bus is "1".

S_1: Starting Position Selector. This specifies the first address in the data transfer. It must be in the range A to P.

S_2: Ending Position Selector. This specifies the last address in the data transfer. It must be in the range A to P and equal to or greater than S_1.

The "I" command specifies the range of data positions to be sequentially output to the system controller by a read operation.

Example:

"I1DF"

I: Selects data transfer direction for the system controller.

1: Auxiliary equipment address.

D: The first element to be transferred is D.

F: The last element to be transferred is F.

Note: Since the read program word cannot address the "A" position, it will be necessary to execute an interrogate command, with a write command specifying the module to be addressed. In the above example, the information can be read from the module in slot 5 by sending "W1AA5I1DF". If the module in slot 5 was the last module to receive a write command, that module should still be selected. It would then suffice to send only the "I" (interrogate command).

In the preceding example, the data contained in positions D, E, and F will be transferred from the module in slot 5 to the controller via the 4 Bit Parallel Bus.

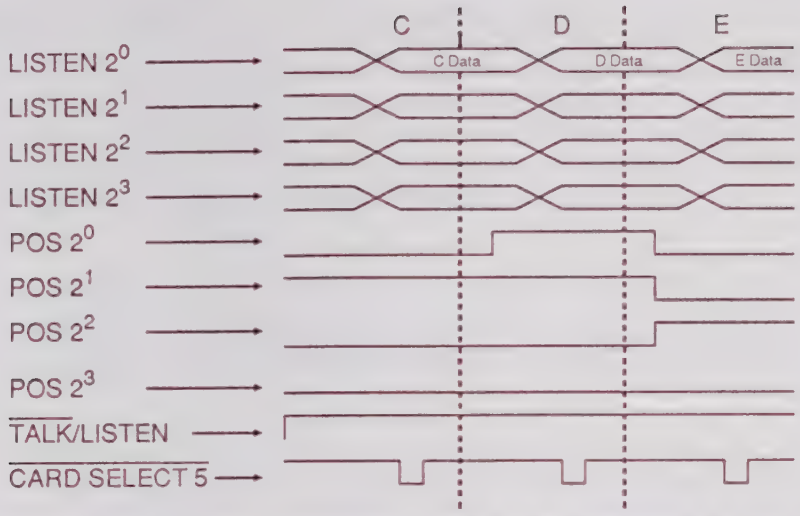


Figure 3.2.3.2 Transmission Sequence on the 4 Bit Parallel Bus in the Listen (Interrogate) Mode.

3.3. Four Bit Parallel Bus Control Expansion Connection

The Four Bit Parallel Bus, also known as the Aux Bus, can be expanded to control instruments which are external to and completely independent of the UTI-1 Universal Test Interface. This is accomplished by connecting all of the Four Bit Parallel Bus lines to Control Expansion Connector BU2. The Control Expansion Connector BU2 is available in both the IEEE-488 Interface module and the Parallel Bus Interface module.

3.3.1 General Hardware Description

The Four Bit Parallel Bus control expansion connection, in conjunction with external Buffer Stores, is used to control fourteen additional instruments having BCD remote control interfaces.

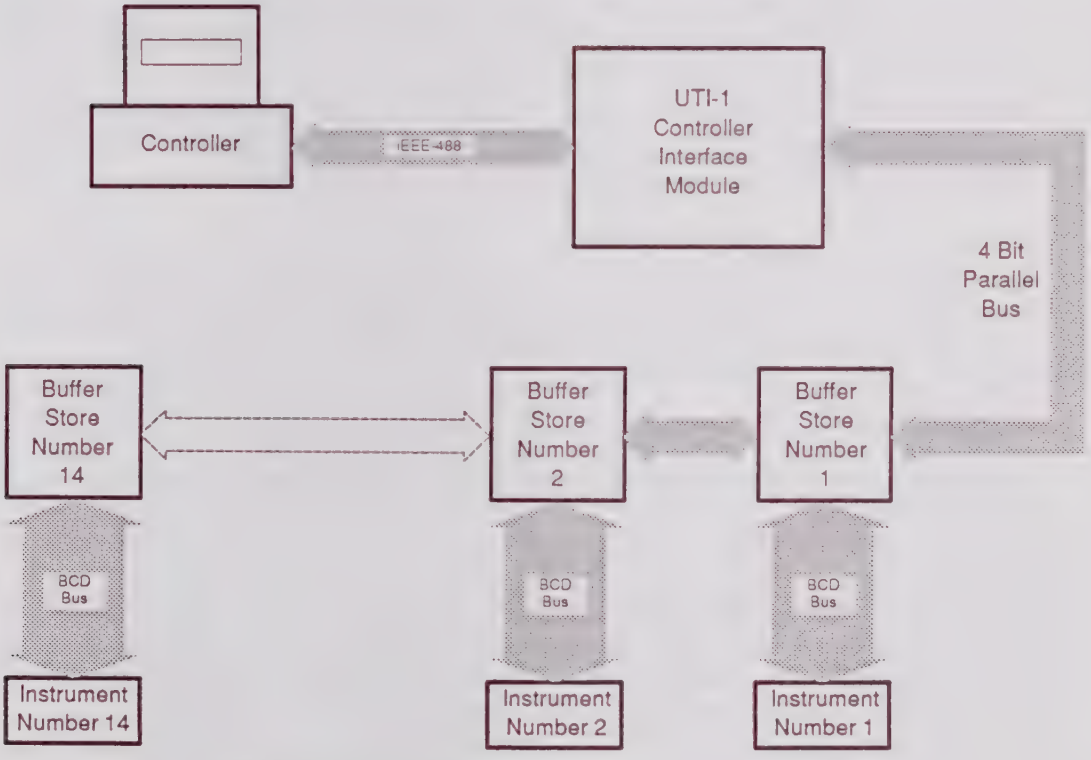


Figure 3.3.1 Instrument Connection Block Diagram

Figure 3.3.1 illustrates the connection of fourteen separate instruments. Data is transmitted in both directions between the controller and the BCD controlled instruments via the controller interface module in the UTI-1 Universal Test Interface.

The controller interface module serves as the format converter for the bidirectional data throughput between the controller and the BCD controlled instruments.

Buffer Stores between the controller interface and the individual instruments are essential for latching the bidirectional BCD parallel data.

UTI-1 Controller Interface Module

Wandel and Goltermann offers two controller interface modules which provide the Four Bit Parallel Bus expansion connection. These are, the IEEE-488 Interface module and the Parallel Bus Interface module.

The Four Bit Parallel Bus is accessed by the Buffer Stores through a 24 pin connector mounted on the rear panel of the controller interface module. Up to fourteen Buffer Stores can be daisy chained from this connector.

Communication via the controller interface module is accomplished by using WRITE control blocks(write to Buffer Stores) and INTERROGATE control blocks (read from Buffer Stores). The WRITE and INTERROGATE control blocks are described in section 3.3.3.

Buffer Stores

Buffer Stores are specialized data latch circuitry used to communicate with instruments which have a parallel BCD control interface. Such instruments can be controlled by providing appropriate logic levels to their remote control lines.

Due to the diversity of BCD controlled instrumentation, Buffer Stores are usually designed for a specific instrument. Generally, they are designed for latching instrument setup data sent by the controller. However, when used with equipment that provides status and measuring reports, Buffer Stores are designed for latching BCD status and result data from the instrument as well.

3.3.2 Four Bit Parallel Bus Lines Description

The Four Bit Parallel Bus is accessed through a 24 pin Amphenol connector on the rear panel of the computer interface module located in slot 0 of the UTI-1 Universal Test Interface. The bus is composed of the following signal lines:

- 2 +15V DC Power lines
- 2 Ground lines
- 4 TALK DATA lines
- 4 LISTEN DATA lines
- 4 DATA POSITION lines
- 4 Auxiliary Equipment Address lines
- 1 $\overline{T}$/L ($\overline{TALK}$/LISTEN) line
- 1 $\overline{REMOTE}$/LOCAL line

Figure 3.3.2 shows a block diagram of the layout of these signal lines.

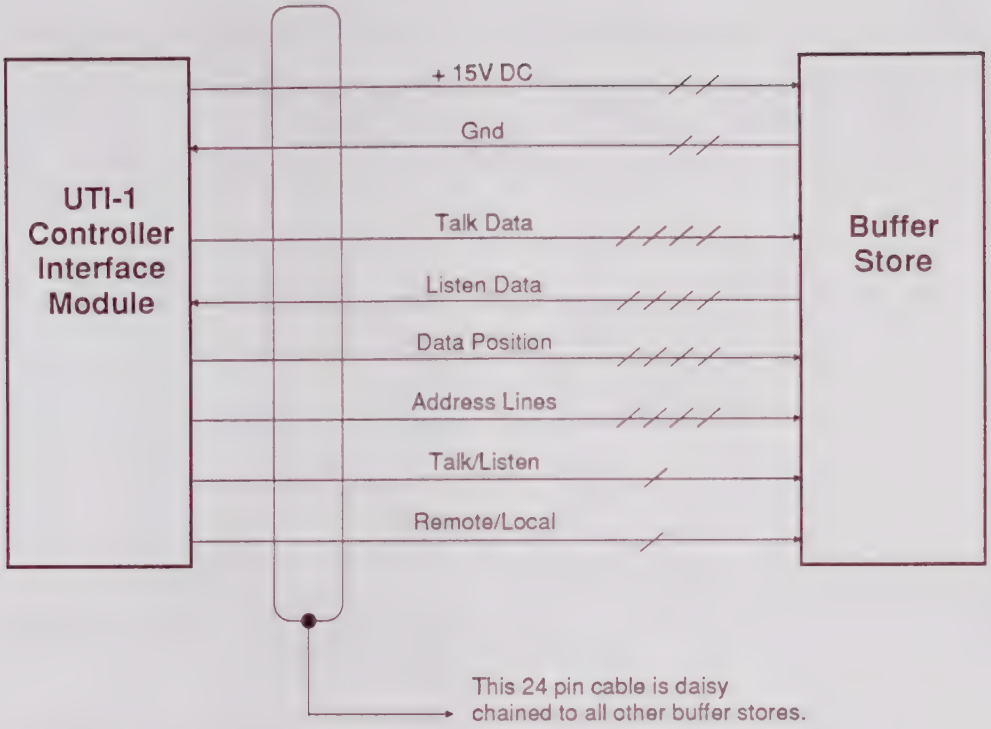


Figure 3.3.2 Four Bit Parallel Bus Block diagram

The +15V DC lines power up all of the connected Buffer Stores. Each Buffer store can be equipped with an on-board 5V regulator.

The Ground lines provide the power return for all of the connected Buffer Stores. The ground must be connected to the Buffer Store and to the controlled instrument as well.

The four TALK DATA lines (TALK 2^0, TALK 2^1, TALK 2^2, TALK 2^3) provide the data to the controlled element. The range of binary data is the ASCII characters 0 through 9, :, ;, <, =, >, and ?. Of the binary data sent from the computer, the four left most digits are stripped off the 8 bit character, and only the four right most digits are evaluated. The logic of these lines is positive true.

The four LISTEN DATA lines (LISTEN 2^0, LISTEN 2^1, LISTEN 2^2, LISTEN 2^3) are used to send data back to the system controller. The range of the binary data is 0 through 15. Data above 9 will be assembled in the controller interface module as ASCII characters :, ;, <, =, >, and ?. The character assembly includes the addition of the four most significant bits to the individual ASCII characters. The logic of these lines is positive true.

The four DATA POSITION lines (POS 2^0, POS 2^1, POS 2^2, POS 2^3) are used to indicate to the addressed Buffer Stores the position of each data character in either WRITE or INTERROGATE control blocks. These lines provide the means of addressing each individual latch within the addressed Buffer Store. Table 3.3.2 shows the binary value for each character position. The logic of these lines is positive true.

Table 3.3.2 Binary Representation of each Character Position

DATA POSITION code 2^3	2^2	2^1	2^0	TALK DATA character
0	0	0	0	A
0	0	0	1	B
0	0	1	0	C
0	0	1	1	D
0	1	0	0	E
0	1	0	1	F
0	1	1	0	G
0	1	1	1	H
1	0	0	0	I
1	0	0	1	J
1	0	1	0	K
1	0	1	1	L
1	1	0	0	M
1	1	0	1	N
1	1	1	0	O
1	1	1	1	P

The T/L line is used to indicate the direction of data in the Four Bit Parallel Bus. During a WRITE control block (talk mode), this line remains low. During INTERROGATE control blocks (listen mode), this line remains high.

The four ADDR lines provide the capability of addressing several Four Bit Parallel Bus instruments. These lines are binary coded and are normally set to binary 1110 (decimal 14). The purpose of these lines is to select a specific instrument within the address range of the Four Bit Parallel Bus. The address assignment for Buffer Stores must conform to Table 3.3.2, which allows a maximum of fourteen (0 through 15 except 1 and 14) separate units to be installed.

Table 3.3.2 Auxiliary Equipment Address Assignment

Addr Bits 2	2	2	2	Decimal Number	Assigned Equipment
0	0	0	0	0	Buffer Store
0	0	0	1	1	UTI-1
0	0	0	2	2 thru 13	Buffer Store
1	1	1	0	14	Reserved for firmware use
1	1	1	1	15	Buffer Store

The $\overline{\text{REMOTE}}$/LOCAL line is set low (remote) or high (local) by the controller via the controller interface module. This line can be used to arm the Buffer Store and, if necessary, to set the controlled instrument in remote or local mode.

3.3.3 Programming Word

Buffer Stores establish the link between the controller and a given instrument using WRITE control blocks and INTERROGATE control blocks. These control blocks consist of a header or word identifier which sets up the Four Bit Parallel Bus Interface in the controller interface module and specifies the direction of data transfer.

The WRITE control block is used to write to devices in the Four Bit Parallel Bus. It contains, in addition to the word specifier, the Auxiliary Equipment Address and setup data for specific instruments.

The INTERROGATE control block is used to read from devices in the Four Bit Parallel Bus. It contains, in addition to the word specifier, the Auxiliary Equipment Address and specific data positions from which data is to be read.

The Auxiliary Equipment Address selects which Buffer Store is to engage in data transfer with the controller.

3.3.3.1 Writing to Buffer Stores

Writing to Buffer Store is done by using WRITE control blocks. The Four Bit Parallel Bus WRITE control blocks have the following format:

OUTPUT 709;"W X S_1S_2 a b c d e f g h i j k l m n o p"

Where:

OUTPUT: Output data statement required by the HP 9000 200/300 series computer.

7: Computer related I/O plug-in (IEEE-488 Interface) address.

09: IEEE-488 Interface Module address.

W: Word identifier "W" identifies the string as a write command.

X: Auxiliary equipment address: An address that is used only by the computer interface module in slot 0 to differentiate between hardware connected to the UTI-1 mother board and the Buffer Stores connected to Control Expansion Connector BU2. The auxiliary equipment address of the UTI-1 motherboard bus is "1".

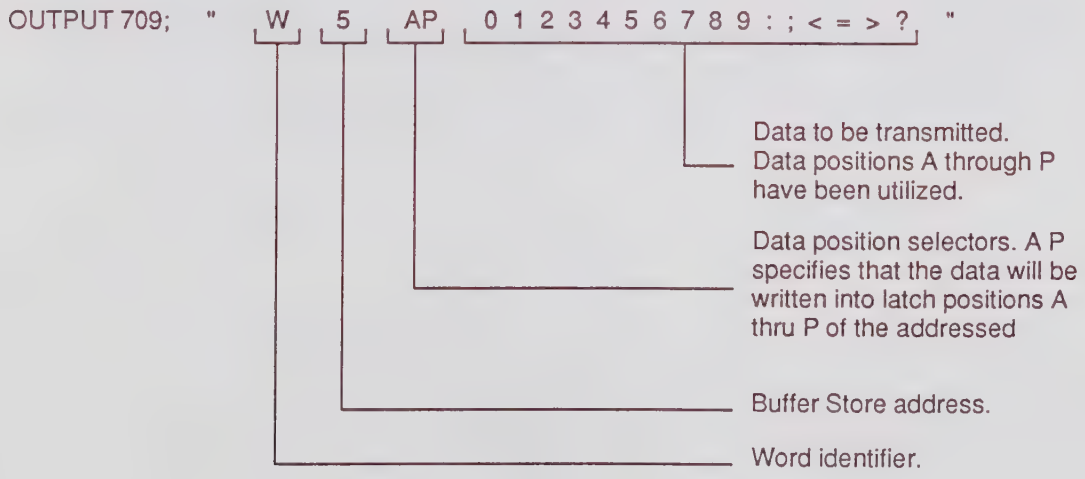
Auxiliary Equipment Addresses for the Buffer Stores must be set to conform to Table 3.3.2.

S_1: Starting Position Selector. This specifies the first address in the data transfer. It must be in the range of A to P.

S_2: Ending Position Selector. This specifies the last address in the data transfer. It must be in the range of A to P and equal or greater than S_1.

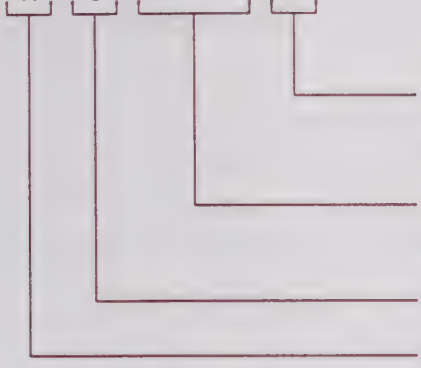
a-p: The actual data to be transferred over the four talk lines. Since there are 16 possible values, each position is coded as one of the 16 consecutive ASCII characters starting with "0" (0123456789:;<=>?). The first character corresponds to the data sent to the address specified in S_1. Each additional character determines the data sent to each successive address until S_2 is reached. The number of data characters must match the range of data positions specified by S_1 and S_2.

Sample 1:



Sample 2:

OUTPUT 709; " W 6 A A 2 "



Data to be transmitted. Only data position A has been utilized.

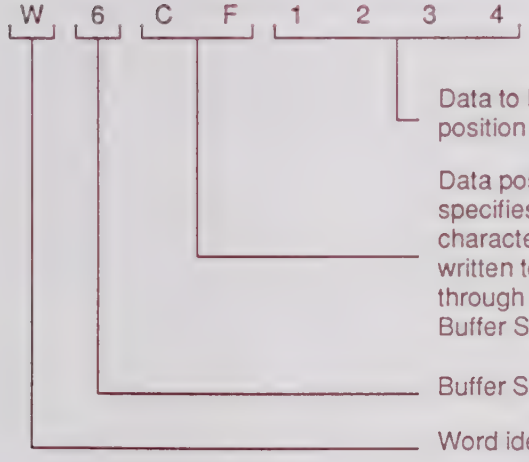
Data position selectors. A A specifies that data character 2 will be written to latch position A of the addressed Buffer Store.

Buffer Store address.

Word identifier.

Sample 3:

OUTPUT 709; " W 6 C F 1 2 3 4 "



Data to be transmitted. Only data position A has been utilized.

Data position selectors. C F specifies that the four data characters (1, 2, 3, 4) will be written to latch positions C through F of the addressed Buffer Store.

Buffer Store address.

Word identifier.

Note: Spaces between each character in the examples above are used for illustrative purposes only.

Sample 4:

OUTPUT 709;"W4AC123W5CD12W3AH12345678"

In the above example, the total string contains three WRITE control blocks. The controller interface module is capable of receiving a string of multiple control blocks.

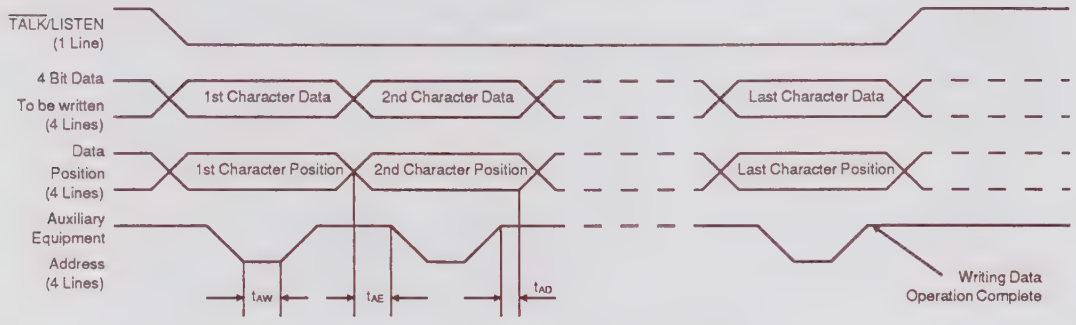


Figure 3.3.3.1 Transmission sequence on the 4-Bit Parallel Bus in the Talk Mode.

Parameter Name		Min.	Max.	Unit
Address Pulse Width	(tAW)	80	120	µSec
Address Enable Delay	(tAE)	40	80	µSec
Address Enable Hold	(tAD)	20	150	nSec
Card Select Delay	(tSE)	2	2.5	µSec
Card Select Width	(tSW)	80	120	µSec

3.3.3.2 Reading from Buffer Stores

Reading from Buffer Stores is done using INTERROGATE control blocks. INTERROGATE control blocks in the Four Bit Parallel Bus are of the following format:

OUTPUT 7 0 9 ; "I X S_1 S_2"

Where:

OUTPUT: Output data statement required by the HP9000 300/200 series computers.

7: Computer related I/O plug-in module (IEEE-488 Interface) address.

09: IEEE-488 Interface Module Address.

I: Identifies the string as a read command.

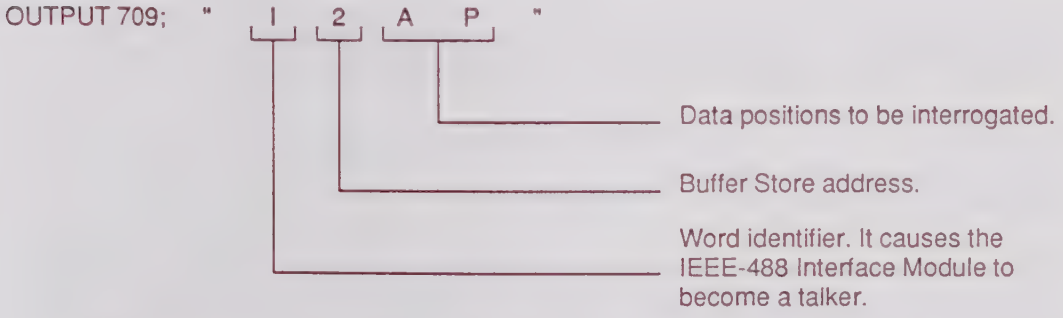
X: Auxiliary equipment address: An address that is used only by the computer interface module in slot 0 to differentiate between 4 Bit Parallel Bus on the motherboard and the Buffer Stores connected to Control Expansion Connector BU2. The auxiliary equipment address of the UTI-1 motherboard bus is "1".

Auxiliary Equipment Addresses for the Buffer Stores must be set to conform to Table 3.3.2.

S_1: Starting Position Selector. This specifies the first address in the data transfer. It must be in the range of A to P.

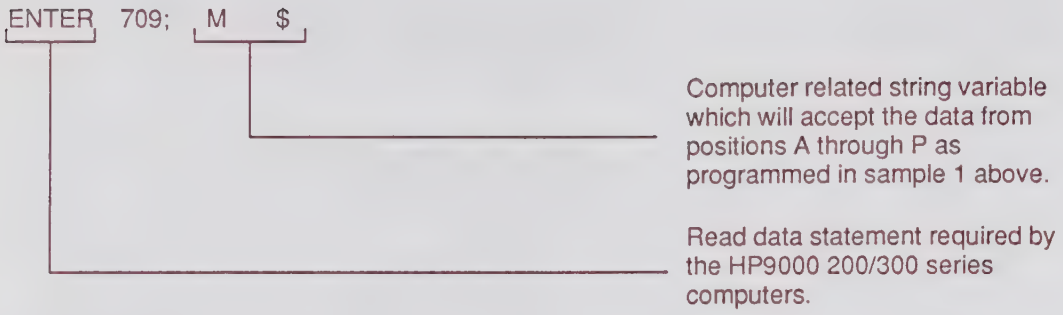
S_2: Ending Position Selector. This specifies the last address in the data transfer. It must be in the range of A to P and equal or greater than S_1.

Sample 1:

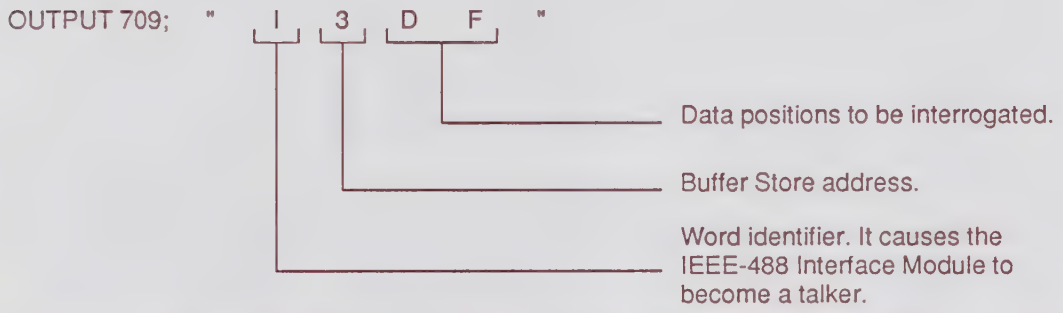


This INTERROGATE control word sets up the controller interface module to become a talker and the Four Bit Parallel Bus interface to transfer data from the Buffer Store to the controller. The actual computer related "READ" statement is shown in sample 2 below.

Sample 2:

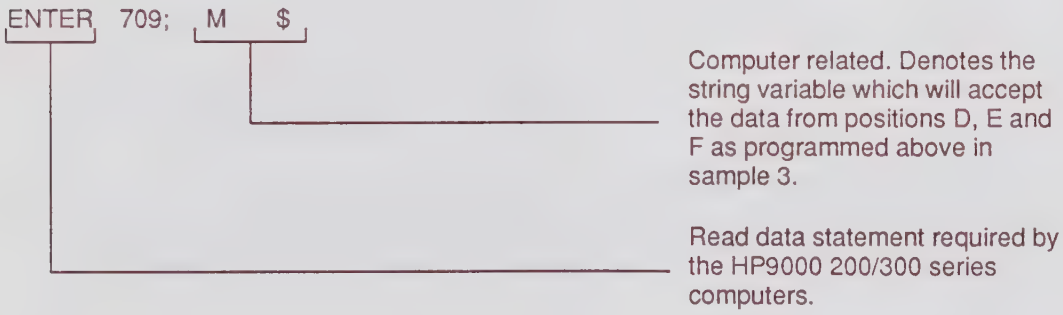


Sample 3:



This word sets up the controller interface module to become a talker and sets up the Four Bit Parallel Bus to transfer data from the addressed Buffer Store to the controller. The actual computer related "READ" statement is shown in sample 4 below.

Sample 4:



This computer READ statement complements example 3 above by fetching characters D and E and placing these characters into string variable M$.

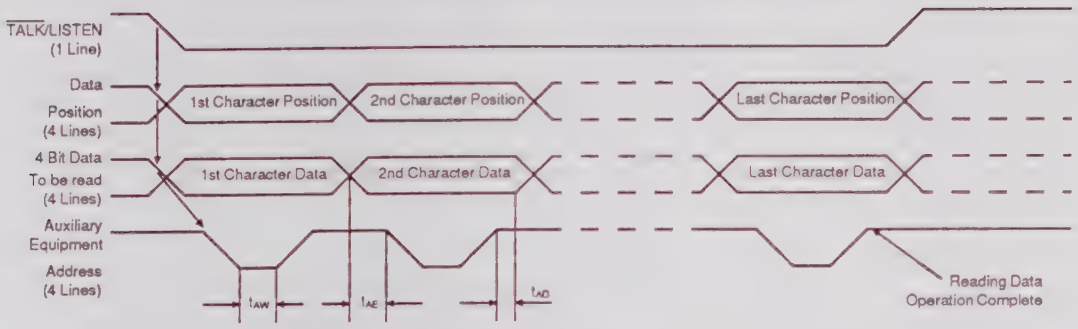


Figure 3.3.3.2 Transmission Sequence on the 4 Bit Parallel Bus in the Listen (Interrogate) Mode.

Parameter Name		Min.	Max.	Unit
Address Pulse Width	(tAW)	80	120	µSec
Address Enable Delay	(tAE)	40	80	µSec
Address Enable Hold	(tAD)	20	150	nSec
Card Select Delay	(tSE)	2	2.5	µSec
Card Select Width	(tSW)	80	120	µSec

3.3.4 Sample Buffer Store

The General Usage Buffer Store BN 9534-8400.33 offered by Wandel and Goltermann can be used to interface with various instruments having a TTL compatible parallel BCD interface.

The General Usage Buffer Store provides sixteen standard output lines and sixteen standard input lines which are permanently wired. Sixteen additional lines are provided with input or output jumper options. All of the instrument signal lines are connected to a 50 pin Amphenol connector.

An on-board voltage regulator provides the appropriate voltage level to the internal circuitry.

Manual/Remote switch S1 is used to manually set the connected instrument to either remote or local mode.

Figure 3.3.4 shows a simplified diagram of the General Usage Buffer Store.

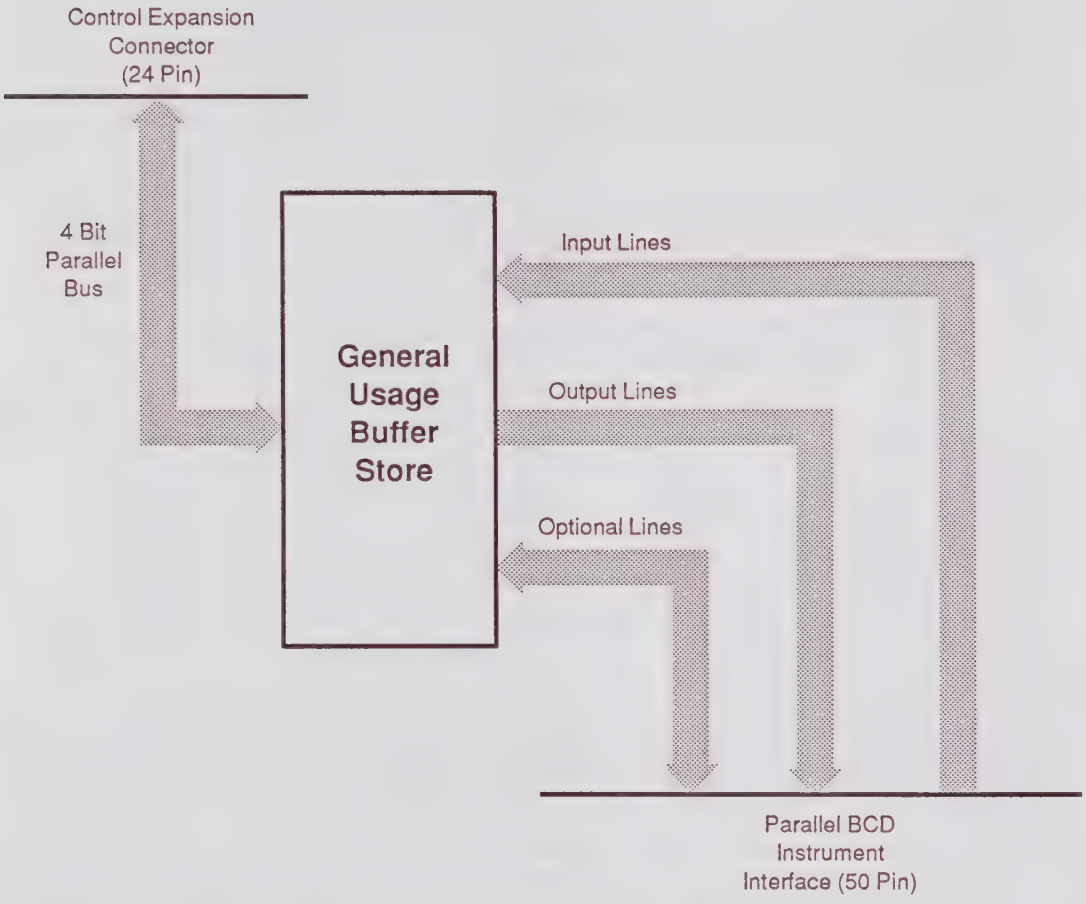


Figure 3.3.4 General Usage Buffer Store Block Diagram

3.3.4.1 Four Bit Parallel Bus Connection

The Four Bit Parallel Bus connection is made via 24 pin Amphenol connector BU1 (refer to schematic drawing). Table 3.3.4.1 lists the pin assignment for BU1.

Table 3.3.4.1 Four Bit Parallel Bus Connector Pin Assignment.

Signal Name	Pin		Signal Name
Data Output 2^0	1	13	Data Output 2^1
Data Output 2^2	2	14	Data Output 2^3
Data Position 2^0	3	15	Data Position 2^1
Data Position 2^2	4	16	$\overline{\text{Talk}}$/Listen
Address 2^0	5	17	Address 2^1
Address 2^2	6	18	Address 2^3
Listen 2^0	7	19	Listen 2^1
Listen 2^2	8	20	Listen 2^3
Data Position 2^3	9	21	NC
NC	10	22	$\overline{\text{Remote}}$/Local
+15V DC	11	23	Ground
+15V DC	12	24	Ground

3.3.4.2 Parallel BCD Instrument Connection

Connection to the instrument is made via 50 pin connector BU2 (refer to schematic drawing). Table 3.3.4.2 lists the pin assignment for BU2.

The standard configuration of the General Usage Buffer Store allows control of four BCD coded signal groups. Each BCD coded signal group is composed of four signal lines representing a single data position character. The four data position characters represented in the General Usage Buffer Store are "A", "B", "C", and "D". Four additional data position character (position characters E, F, G, and H) can be implemented by linking the appropriate jumper option connections.

The General Usage Buffer Store provides several on board jumper option connections in order to accommodate a wide variety of applications.

Address Select Jumpers

For address range 0 to 9 connect point S to point T.

For address range 10 to 15 (except 14) connect point S to point U, and point V to point T.

Connect resistor R3 to the output pin of IC7 that corresponds the desired Buffer Store address. For example, to select Buffer Store address 7 connect R3 to pin 9 of IC7. Note that for address range 10 to 15 (except 14) only decimal decoded outputs 0 through 5 of IC7 (pins 1 through 6) must be used.

Input Logic

For positive input logic connect the following jumpers:

1. Point W to point Y (output of IC2)
2. Point Z to point AB (output of IC5)
3. Point AC to point AD (output of IC8)
4. Point AF to point AH (output of IC11)
5. All unused inputs should be set to logic zero.

For negative input logic connect the following jumpers:

1. Point X to point Y (output of IC2)
2. Point AA to point AB (output of IC5)
3. Point AE to point AD (output of IC8)
4. Point AG to point AH (output of IC11)
5. All unused inputs should be set to logic one.

Output Logic

For positive output logic connect point AK to point AJ (input of IC13).

For negative output logic connect point AK to point AI (input of IC13).

Optional Inputs

In the standard configuration, the General Usage Buffer Store allows the input of four BCD coded characters (data position characters A, B, C, and D). One more BCD coded input character (data position character E) can be readily implemented at the General Usage Buffer Store instrument connection by linking the following jumpers:

1. Point A (BU2 pin 37) to point B
2. Point C (BU2 pin 38) to point D
3. Point E (BU2 pin 39) to point F
4. Point G (BU2 pin 40) to point H

Optional Outputs

In the standard configuration, the General Usage Buffer Store allows the output of four BCD coded characters (data position characters A, B, C, and D). One more BCD coded output character (data position character E) can be readily implemented at the General Usage Buffer Store instrument connection by linking the following jumpers:

1. Point J (BU2 pin 17) to point I
2. Point L (BU2 pin 18) to point K
3. Point N (BU2 pin 19) to point M
4. Point P (BU2 pin 20) to point R

Unassigned I/O Pins

Pins 41 through 45 and 47 through 49 of BU2 are eight unassigned I/O lines which can be configured as either inputs or outputs.

Pins 12 through 14 of IC2, IC5, IC8, and IC11 are reserved for optional inputs lines.

Pins 10 through 12 of IC3, IC6, IC9, and IC12 are reserved for optional output lines.

The following two examples illustrate the addition of data position characters to both input and output ports.

Sample 1: To implement input data position character G, connect the following jumpers:

1. Point OP1 (BU2 pin 41) to pin 14 of IC2
2. Point OP2 (BU2 pin 42) to pin 14 of IC5
3. Point OP3 (BU2 pin 43) to pin 14 of IC8
4. Point OP4 (BU2 pin 44) to pin 14 of IC11

Sample 2: To implement output data position character H, connect the following jumpers:

1. Point OP5 (BU2 pin 45) to pin 12 of IC3
2. Point OP6 (BU2 pin 47) to pin 12 of IC6
3. Point OP7 (BU2 pin 48) to pin 12 of IC9
4. Point OP8 (BU2 pin 49) to pin 12 of IC12

Table 3.3.4.2 50 Pin Amphenol Connector Pin Assignment

Signal Name	Pin		Signal Name
Output 2^0 Byte A	1	26	Input 2^1 Byte B
Output 2^1 Byte A	2	27	Input 2^2 Byte B
Output 2^2 Byte A	3	28	Input 2^3 Byte B
Output 2^3 Byte A	4	29	Input 2^0 Byte C
Output 2^0 Byte B	5	30	Input 2^1 Byte C
Output 2^1 Byte B	6	31	Input 2^2 Byte C
Output 2^2 Byte B	7	32	Input 2^3 Byte C
Output 2^3 Byte B	8	33	Input 2^0 Byte D
Output 2^0 Byte C	9	34	Input 2^1 Byte D
Output 2^1 Byte C	10	35	Input 2^2 Byte D
Output 2^2 Byte C	11	36	Input 2^3 Byte D
Output 2^3 Byte C	12	37	Optional Input
Output 2^0 Byte D	13	38	Optional Input
Output 2^1 Byte D	14	39	Optional Input
Output 2^2 Byte D	15	40	Optional Input
Output 2^3 Byte D	16	41	Optional Input/Output
Optional Output	17	42	Optional Input/Output
Optional Output	18	43	Optional Input/Output
Optional Output	19	44	Optional Input/Output
Optional Output	20	45	Optional Input/Output
Input 2^0 Byte A	21	46	Remote/Manual
Input 2^1 Byte A	22	47	Optional Input/Output
Input 2^2 Byte A	23	48	Optional Input/Output
Input 2^3 Byte A	24	49	Optional Input/Output
Input 2^0 Byte B	25	50	Ground

3.4. Sixteen Bit Parallel Bus

The 16 bit parallel bus is one of the two busses permitting communication between the system controller and the UTI-1 modules. The other bus is a 4 bit parallel bus (also known as the Aux Bus). Of the two available computer interfaces, the IEEE Interface module supports only the Four Bit Parallel Bus. With the appropriate software, the Parallel Bus Interface module supports both the Four Bit Parallel Bus and the 16 Bit Parallel Bus.

To provide testing flexibility, UTI-1 modules have controllable elements such as relays, logic circuits and microprocessors. The system controller, together with the operating program, transmits control data to these elements. A program statement is used to address, change, and read the status of the element. In addition, the parallel bus signals are also available on the ITA from the Parallel Bus Interface Module. These are used to control the device under test and to pass data between the device under test and the system controller.

3.4.1 General Description

The sixteen bit parallel bus is essentially an extension of the internal address data bus (DIO bus) from the HP 9000 series 200/300 computers. The interface circuitry on the Parallel Bus Extender Module and the Parallel Bus Interface module allows data transfer between the system controller and the UTI-1 modules or test object on the ITA (Interchangeable Test Adapter). The address/data bus in the UTI-1 motherboard and the ITA is called the 16 bit parallel bus in this document.

The Parallel Bus Extender Module is inserted in one of the computer I/O slots, and the Parallel Bus Interface is inserted in slot 0 of the UTI-1. The Extender Module connects the DIO bus signals to the Parallel Bus Interface in the UTI-1 through a 50 pin cable. The Parallel Bus Interface then provides the signals to the ITA through the 64 pin front connector Bu 1 and to the UTI-1 modules through the UTI-1 motherboard connections.

The software for controlling modules using the Sixteen Bit Parallel Bus can be written either in BASIC or Assembler. Driver routines to program the parallel bus extender and Parallel Bus Interface modules are available. These routines facilitate the use of the Sixteen Bit Bus to control the UTI-1 modules.

3.4.2 Sixteen Bit Parallel Bus Line Descriptions

The Parallel Bus Interface Module in slot 0 controls the transfer of data. A description of the parallel bus lines follows:

* The R/$\overline{W}$ (read/$\overline{write}$) line connects from the Parallel Bus Interface Module in slot 0 to the other 15 slots via the UTI-1 motherboard. The state of this single line indicates the direction of data transfer. This line is unidirectional and driven by the Parallel Bus Interface Module.
* The 15 card select lines ($\overline{CS1}$ through $\overline{CS15}$) connect the Parallel Bus Interface Module in slot 0 to one of the other slots (1 through 15) via the UTI-1 motherboard. Only the selected card should respond to the parallel bus signals. These lines are unidirectional and are driven by the Parallel Bus Interface Module.

* The 16 bidirectional data lines (D_0 - D_{15}) are used for data transfer and are driven either by a UTI-1 module or by the Parallel Bus Interface Module, depending upon the direction of data transfer. These lines can be active in groups of 8 bits (D_0 to D_7 or D_8 to D_{15}) or as one group of all 16 bits.
* The 15 unidirectional address lines (A_1 - A_{15}) are used for accessing locations in a UTI-1 module. There is no A_0 line. Address line A_0 is implied depending upon the active data strobe. All odd addresses correspond to the lower data bytes D_0 to D_7 and all even addresses to the upper data bytes D_8 to D_{15}.
* The Address Strobe ($\overline{ADS}$) is unidirectional and is under the control of the Parallel Bus Interface Module. When it is low, this line indicates that the address lines are valid.
* The Data Strobes ($\overline{LDS}$ and $\overline{UDS}$) are unidirectional and are under the control of the Parallel Bus Interface module. The lower data strobe ($\overline{LDS}$) is active if data access is on lines D_0 to D_7. Upper data strobe ($\overline{UDS}$) is active during access on lines D_8 to D_{15}. Both the strobes are active for 16 bit data access.
* Interrupt Request ($\overline{IR}$) is an open collector line. Any UTI-1 module can pull this line low to interrupt the system controller.
* Data Transfer Acknowledge ($\overline{DTACK}$) is unidirectional. The UTI-1 module uses this line to acknowledge data transfer.

Note: The ITA can access all of the above lines except for the card selects.

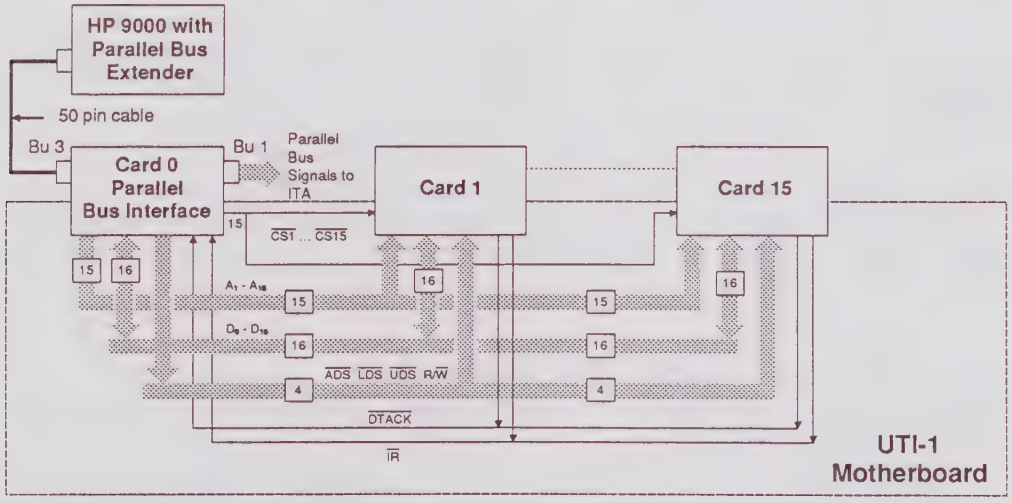


Figure 3.4.2 16 Bit Parallel Bus

3.4.3 16 Bit Parallel Bus Operation

In bus nomenclature, the UTI-1 Parallel Bus Interface Module is called the bus master. Any other UTI-1 module, or the Unit Under Test on the ITA operating on the parallel bus, is called a bus slave.

The UTI-1 parallel bus interface can be programmed to select as a bus slave either the Unit Under Test or, using the card select lines, a UTI-1 module. Only the module selected as a bus slave will respond to the bus signals.

3.4.3.1 Overview of Read/Write Operation

The read/write cycle begins when $\overline{ADS}$ appears on the parallel bus, indicating that address A_1 to A_{16} is valid. A high on the R/$\overline{W}$ line indicates a read cycle, and a low indicates a write cycle. $\overline{UDS}$ and $\overline{LDS}$ indicate whether the upper (D_8 - D_{15}), lower (D_0 - D_7), or both data bytes participate in the cycle.

An interlocked handshake coordinates the data transfer between the bus master and the selected bus slave. $\overline{DTACK}$ (Data Transfer Acknowledge) is the signal returned by the bus slave after having accepted data from or provided data to the bus. The handshake sequence is as follows:

1. Bus master asserts A_1 - A_{15}, $\overline{ADS}$, R/$\overline{W}$, and one or two data strobes. Data Bus signals D_0 - D_7 and or D_8 - D_{15} are also asserted for write cycles.
2. Bus slave asserts $\overline{DTACK}$ when data has been accepted (write cycle) or valid data has been placed on the bus (read cycle) by the slave.
3. Bus master clears $\overline{ADS}$ and data strobes when $\overline{DTACK}$ is recognized (cycle complete). During read cycles, the Bus Master accepts the Data before clearing the strobes.
4. Bus Slave clears $\overline{DTACK}$ when it recognizes that $\overline{ADS}$ or the data strobes are disabled. The data strobe/$\overline{DTACK}$ handshake is necessary to accommodate the varying response times encountered when dealing with a variety of bus slaves. Response times of a given slave can also vary, such as when memory access is requested during a memory refresh cycle.

Read Cycle Description

In the following discussion $\overline{DS}$ refers to either $\overline{UDS}$ and/or $\overline{LDS}$ signals combined. The sequence of events during a read cycle is as follows:

1. Prior to initiating a read cycle, the Bus Master forces $\overline{ADS}$, R/$\overline{W}$, $\overline{UDS}$, and $\overline{LDS}$ high. The $\overline{DTACK}$ line is pulled high by the termination network on the bus master.
2. The bus master drives the address bus lines A_1 to A_{15}. The specific address code is valid at least 20 nsec before $\overline{ADS}$ goes low. The bus master also drives $\overline{DS}$ low. The R/$\overline{W}$ becomes high at least 40 nsec before $\overline{DS}$ are strobed low (setup time).
3. The bus slave places the requested data on the bus after $\overline{DS}$ is asserted. The bus slave then asserts $\overline{DTACK}$ indicating that data signals are valid. The time delay from DS to data valid is device dependent. Data must be valid on every line of the data bus at least 15 nsec before $\overline{DTACK}$ is valid. The bus slave must respond with $\overline{DTACK}$ within 2 nsec after $\overline{DS}$ and $\overline{ADS}$ have become active to prevent bus error.
4. When the bus master recognizes $\overline{DTACK}$ it ends the cycle by clearing $\overline{DS}$ and $\overline{ADS}$.
5. The bus slave clears $\overline{DTACK}$ when it senses that either $\overline{DS}$ or $\overline{ADS}$ has been cleared (this indicates that the cycle is complete).

Write Cycle Description

In the following discussion $\overline{DS}$ refers to either $\overline{UDS}$ and/or $\overline{LDS}$ signals combined. The sequence of events during a write cycle is as follows:

1. Prior to initiating a write cycle, the bus master forces $\overline{ADS}$, R/$\overline{W}$, $\overline{UDS}$, and $\overline{LDS}$ high. The DTACK line is pulled high by the termination network on the bus master.
2. The bus master drives the address bus lines A_1 to A_{15}. The specific address code is valid at least 20 nsec before $\overline{ADS}$ goes low.
3. The bus master places the data on the bus and drives $\overline{DS}$ low. Data is valid on the data bus at least 15 nsec before $\overline{DS}$ is asserted. The R/$\overline{W}$ line is pulled low by the bus master at least 40 nsec before $\overline{DS}$ is low (setup time).

Note: To avoid bus conflicts, do not qualify R/$\overline{W}$ with $\overline{ADS}$. R/$\overline{W}$ is guaranteed to be valid prior to $\overline{DS}$, but may not be valid before ADS goes true.

4. The bus slave stores the data an asserts $\overline{DTACK}$ indicating to the bus master that the data has been accepted.
5. When the bus master detects that $\overline{DTACK}$ is true, it clears $\overline{DS}$ and $\overline{ADS}$. In addition, the bus master removes the data from the data bus. To ensure that the data hold time is sufficient to allow the bus slave to clock the data at the same time as it asserts $\overline{DTACK}$, the Bus master does not disturb the data on the bus for at least 90 nsec after $\overline{DTACK}$ is received from the slave. Shortly after this time (90ns), the data on the bus will become invalid. The bus slave must respond with $\overline{DTACK}$ within 2 sec after $\overline{DS}$ and $\overline{ADS}$ have become active to prevent bus error.

3.4.3.2 Bus Time Outs

The HP computer expects an addressed slave to respond within an established time limit. The bus slaves respond to address sequences from the bus master by activating $\overline{DTACK}$. The bus slave should respond with $\overline{DTACK}$ within 2 μsec of the data and address strobes becoming active. Otherwise, the system controller will begin exception processing.

3.4.3.3 Address Range Assignment

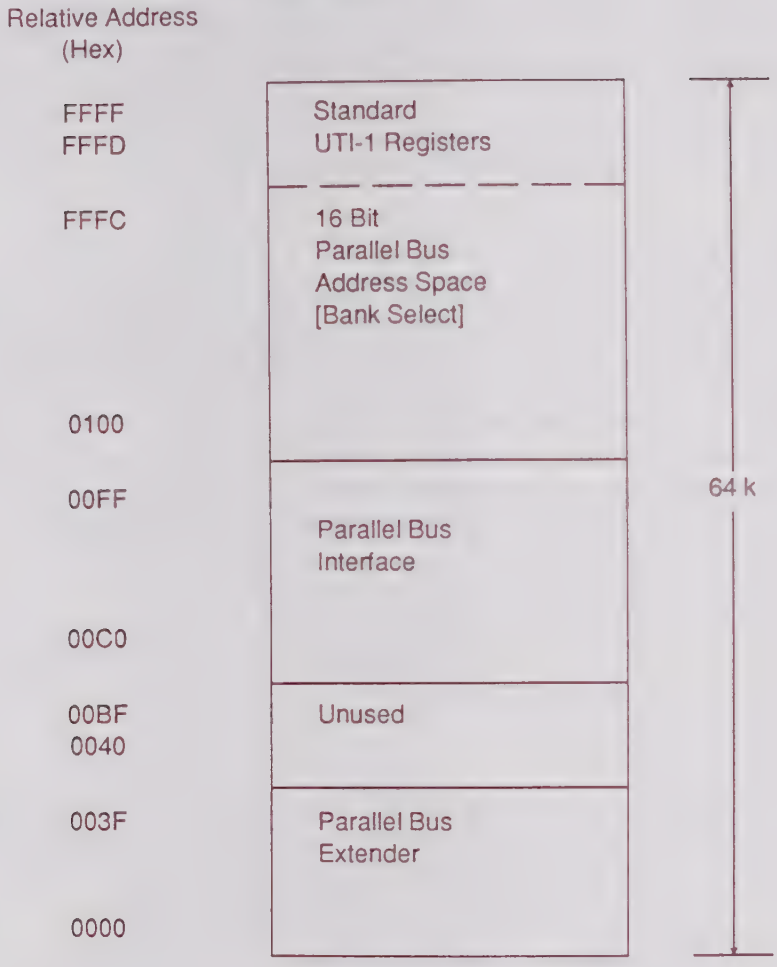


Figure 3.4.3.3 Address Range Assignments

Each I/O card in the HP9000 computer has an alloted address space of 64k. The Parallel Bus Extender, the Parallel Bus Interface and the UTI-1 modules operating on the 16 bit parallel bus have to map into this address space. The 64k absolute address range depends on the select code switch settings on the I/O card.

Figure 3.4.3.3 shows address space assignment within this 64k I/O addressing range. The Parallel Bus Interface Module responds to relative addresses between 00C0 and 00FF. The parallel bus extender module responds to relative addresses between 0000 and 003F. Addresses in the range 0100 to FFFF are available to the UTI-1 modules operating on the 16 bit parallel bus, and to the test object on the ITA. By using Bank Select, both the UTI-1 modules and test object can respond to addresses between 0100 and FFFF, giving each bus slave approximately 63.7k addressing capability. The card select lines are used to bank select the UTI-1 modules. Bank selection is done by programming the Parallel Bus Interface Module.

The UTI-1 modules and the test object on the ITA should be designed to respond only to the relative addresses shown in figure 3.4.3.3.

It is important to note that the parallel bus uses a 16 bit, word oriented (rather than byte wide) architecture, so bit 0 (A_0 of the address) does not appear on the bus. Instead, it is converted into upper and lower byte data strobe signals. When A_0 is "0" during byte read/write transfers, the upper data strobe is asserted. When A_0 is "1", the lower data strobe is asserted. During word transfers, both data strobes are asserted simultaneously. Words are accessed on even addresses, corresponding to the high order byte. The low order byte has an odd address, one byte higher than the word address.

3.4.4 Absolute Addresses

For the HP 9000 Series computers, the External I/O select space begins at address 600000. Each I/O card has 64k byte addresses within the external I/O space. The absolute 64k address range for a I/O card depends upon its select code switch setting. To access a parallel bus slave or to program the Parallel Bus Extender or Parallel Bus Interface Modules, the 24 bit absolute addresses must be known. The absolute address depends on the select code switch settings on the Parallel Bus Extender. A 5 bit switch in the extender allows select codes between 0 to 31 to be set. Each I/O card on the HP 9000 computer is set to a unique select code. The following method is used to find the absolute address.

Absolute address in Hex

= 600000 + Select code x 10000 + relative address

Since the select code switch setting for the Parallel Bus Extender Module is 15 decimal:

Absolute address in Hex

= 600000 + F0000 + relative address
= 6F0000 + relative address

If the assembler is used for software development, then the 24 bit absolute address has to be used. The programming sheets specify the relative addresses only. The assembler code can use address 6F0000 as the base, with all accesses relative to it.

3.4.5 Standard UTI-1 Module Registers

All UTI-1 modules operating on the 16 bit parallel bus must have certain standard registers which are connected to the lower byte of the data bus. The designer is free to implement registers in addition to (but not instead of) the ones listed below. Also, the designer is not required to uniquely map each register to a location within the card's address space (i.e. several addresses may access the same register), which simplifies address decoding, as long as the addresses are not outside the card's address space (relative address 0100 to FFFF of the selected module). The standard registers are not required for the ITA.

Card ID: Relative address FFFF

This address contains the unique card ID for the UTI-1 module. It is preferable to hardwire the card ID. Customers should only use ID numbers E0 through FE, as other card ID numbers are reserved for the standard modules supplied by Wandel & Goltermann.

Bit	7	6	5	4	3	2	1	0
	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

Module Reset: Relative address FFFF

Writing any value into this register resets the UTI-1 module. The response of the card will depend on its design. The module may or may not respond to a write to this register.

A module can also use the RESET line on the motherboard to reset itself. See the description of the Parallel Bus Interface module to determine the conditions under which the RESET line is pulsed. Writing to relative address FFFF does not pulse this line. The RESET line is used as a common reset for all the UTI-1 modules.

Module Status: Relative address FFFD

Bit	7	6	5	4	3	2	1	0
	Undefined						IR	IE

IE Interrupts Enabled: If this bit is set, then interrupts are enabled.

IR Interrupt Request: This bit is used by software polling to determine the origin of the interrupt. If this bit is set, the card is requesting an interrupt.

The UTI-1 module should remove its interrupt request when it detects that its interrupt has been serviced.

Module Control: Relative address FFFD

Bit	7	6	5	4	3	2	1	0
	Undefined							EI

EI Enable Interrupts: Setting this bit enables interrupts.

Undefined These bits have no standard functions and may be defined by the user.

Although UTI-1 modules are not required to have interrupt capability, the bits in the control and status register must be used as defined above.

3.5. Support Information

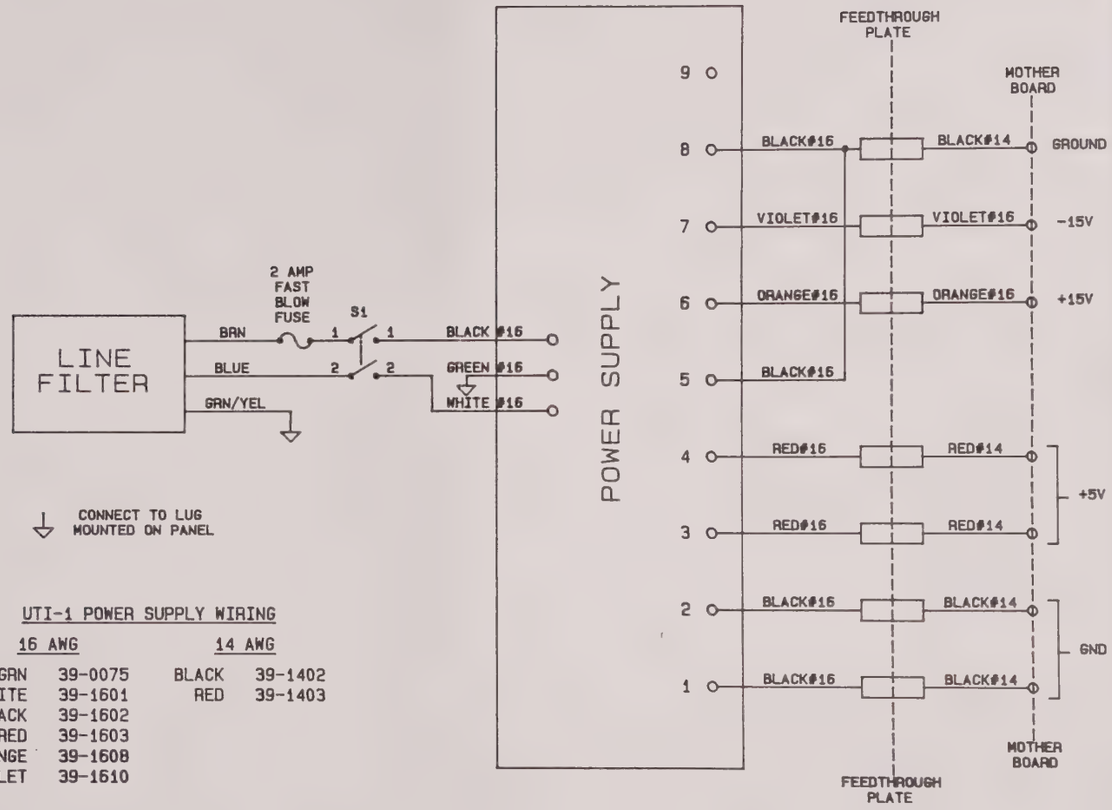
3.5.1. Circuit Description

3.5.1.1 Power Supply

Two different types of power supplies are used in the UTI-1. In series A through C, a 75 watt supply is used, and in series D and up, a 175 watt supply is used. Each of these supplies provides +5 volts, -15 volts, and +15 volts to the motherboard.

3.5.1.2 Fan Circuits

The motherboard contains four fan circuits. Only one fan circuit is presently used; it is connected to the power supply cooling fan. In series A through C, fan circuit 2 is used, and in series D and up, fan circuit 1 is used. The three unused fan circuits are for future use.



UTI-1 POWER SUPPLY WIRING

16 AWG		14 AWG	
GRN	39-0075	BLACK	39-1402
WHITE	39-1601	RED	39-1403
BLACK	39-1602		
RED	39-1603		
ORANGE	39-1608		
VIOLET	39-1610		

NOTE:
THIS WIRING IS VALID ONLY FOR THE 75 WATT POWER SUPPLY XX12-0013, UTI-1 SERIES A-C.

THIS DRAWING IS OUR PROPERTY. IT IS NOT TO BE COPIED OR USED WITHOUT THE WRITTEN CONSENT OF:
WANDEL & GOLTERMANN, INC.

REV	ECN-NO	DATE	NAME
1	NEW	27-7-87	L M G

	NAME	DATE
DRAWN	GARRETT	30-7-87
CHKD	CLS	27-10-87
APPRVD		

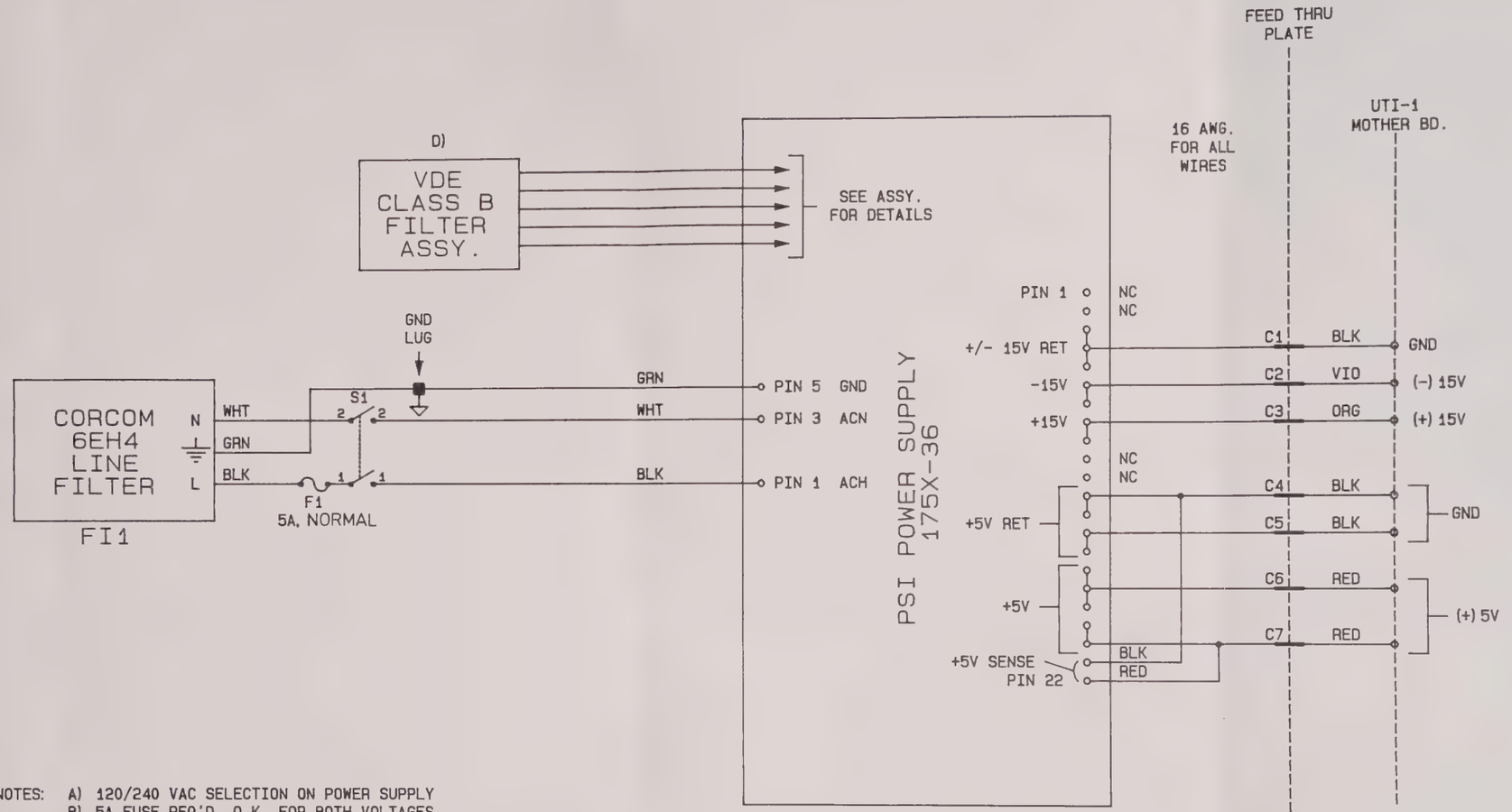
REPLACES
REPLCD BY 9537-7500.02 rev1

UTI-1 POWER SUPPLY WIRING

SERIES A...C

9537-7505.01/B

PG 1 OF 1



NOTES:
A) 120/240 VAC SELECTION ON POWER SUPPLY
B) 5A FUSE REQ'D, O.K. FOR BOTH VOLTAGES
C) LABEL REAR PANEL APPROPRIATELY
D) VDE CLASS B FILTER ASSY. MOUNTED SEPERATELY DUE TO HEIGHT RESTRICTIONS IN POWER SUPPLY HOUSING.

IMPORTANT:

THIS SCHEMATIC APPLIES TO SERIES D UTI-1 AND UP.

FOR SERIES A→C UTI-1 REFER TO 9537-7505.01

REV	ECN-NO	DATE	NAME
1	NEW		M.R.M.
2	88-117	9-SEP-88	

	DATE	NAME
DRAWN	9-8-87	SCHILLER
CHKD		
APPRVD		

REPLACES 9537-7505.01 rev1
REPLCD BY

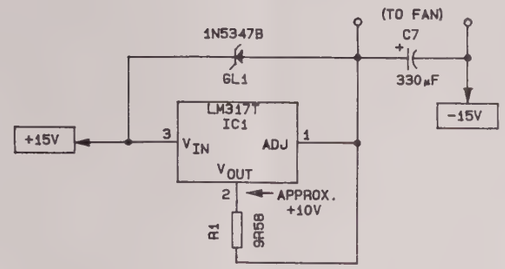
THIS DRAWING IS OUR PROPERTY. IT IS NOT TO BE COPIED OR USED WITHOUT THE WRITTEN CONSENT OF:
WANDEL & GOLTERMANN, INC.

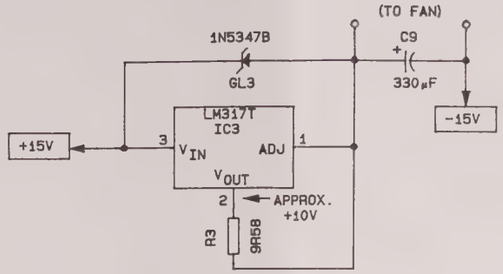
WIRING DIAGRAM FOR PSI175 POWER SUPPLY UTI-1

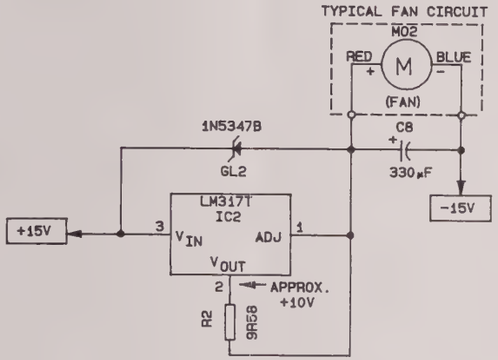
SERIES D...

9537-7505.02/B

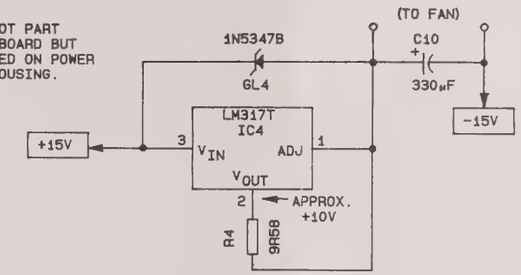
PG 1 OF 1

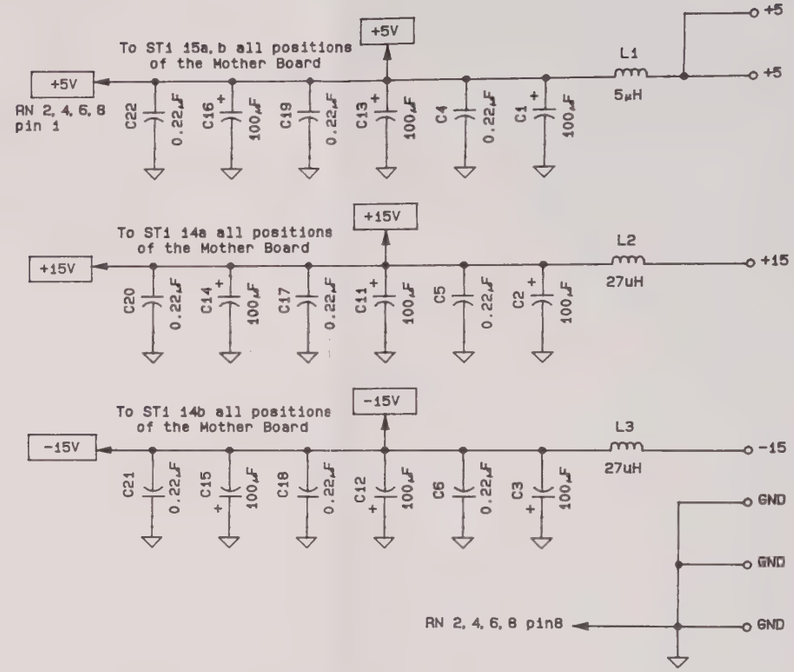






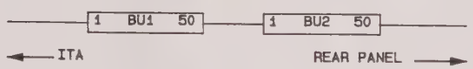
NOTE:
MO2 IS NOT PART OF P.C. BOARD BUT IS MOUNTED ON POWER SUPPLY HOUSING.





NOTES: (APPLICABLE FOR 9537-7508.01 PG.4 & PG.5)

[1] BU1 IS TOWARDS FRONT. BU2 IS TOWARDS REAR.



[2] THESE LINES AVAILABLE ON MOTHER BOARD ONLY IF JUMPERS ARE INSTALLED ON ANALOG MODULE.

[3] CARD SELECT LINES ONLY ON SLOT-0 WHICH IS RESERVED POSITION FOR IEEE 488 CONVERTER MODULE.
CLOCK-1 TO CLOCK-4 NOT AVAILABLE ON SLOT-0.
LOOP BACK SIG-1 AND LOOP BACK SIG-2 NOT AVAILABLE ON SLOT-0.
G-CH1 I.E. PATTERN GENERATOR CH-1 NOT AVAILABLE ON SLOT-0.

9537-J

THIS DRAWING IS OUR PROPERTY.
IT IS NOT TO BE COPIED OR USED
WITHOUT THE WRITTEN CONSENT OF:
WANDEL & GOLTERMANN, INC.

	NAME	DATE	ECN-NO	REV
DRAWN	MEH	26 AUG 87	NEW	1
CHKD				
APPRVD				

REPLACES
REPLCD BY 9537-7508.02 rev1

UTI-1 MOTHER BOARD
POWER CIRCUITS

SERIES A...C

9537-7508.01/B

PG 1 OF 5

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
A/V-2	1B					1B					1B				1B	
A/V-3	2A					2A					2A				2A	
A/V-2/3R	2B					2B					2B				2B	
	3A					3A					3A				3A	
AV-1 (+75V)	3B					3B					3B				3B	
AV-1Q (+75V RETURN)	4A					4A					4A				4A	
AV-41 (RINGING AC H)	4B					4B					4B				4B	
AV-42 (RINGING AC L)	5A					5A					5A				5A	
AV-51 (RINGING DC +)	5B					5B					5B				5B	
AV-52 (RINGING DC −)	6A					6A					6A				6A	
V1 (+)	6B					6B					6B				6B	
V1 (−)	7A					7A					7A				7A	
V2 (+)	7B					7B					7B				7B	
V2 (−)	8A					8A					8A				8A	
V3 (+)	8B					8B					8B				8B	
V3 (−)	9A					9A					9A				9A	
V4 (+)	9B					9B					9B				9B	
V4 (−)	10A					10A					10A				10A	
V5 (+)	10B					10B					10B				10B	
V5 (−)	11A					11A					11A				11A	
V6 (+)	11B					11B					11B				11B	
V6 (−)	12A					12A					12A				12A	
V7 (+)	12B					12B					12B				12B	
V7 (−)	13A					13A					13A				13A	
V8 (+)	13B					13B					13B				13B	
V8 (−)	14A					14A					14A				14A	+15V
+15V	14B					14B					14B				14B	−15V
−15V	15A					15A					15A				15A	+5V
+5V	15B					15B					15B				15B	+5V
+5V	16A					16A					16A				16A	
A/C-2 (ZERO XING +VE IN)	16B					16B					16B				16B	
A/C-3 (ZERO XING −VE IN)	17A					17A					17A				17A	
A/C-4 (ZERO XING LOW LEVEL IN)	17B					17B					17B				17B	
A/C-5 (ZERO XING OUT)	18A					18A					18A				18A	
A/C-1 (INTERLOCK)	18B					18B					18B				18B	
A/C-6 (SUMMING AMP OUT)	19A					19A					19A				19A	
GROUND	19B					19B					19B				19B	GROUND
GROUND	20A					20A					20B				20A	GROUND
GROUND	20B					20B					20B				20B	
INTERCONNECT BUS-1	21A					21A					21A				21A	
INTERCONNECT BUS-2	21B					21B					21B				21B	
GROUND	22A					22A					22A				22A	
GROUND	22B					22B					22B				22B	
INTERCONNECT BUS-1 RETURN	23A					23A					23A				23A	
INTERCONNECT BUS-2 RETURN	23B					23B					23B				23B	
GROUND	24A					24A					24A				24A	
GROUND	24B					24B					24B				24B	GROUND
AUX DMM BUS-1 (+)	25A					25A					25A				25A	
AUX DMM BUS-2 (+)	25B					25B					25B				25B	
GROUND	26A					26A					26A				26A	
GROUND	26B					26B					26B				26B	GROUND
AUX DMM BUS-1 (−)	27A					27A					27A				27A	
AUX DMM BUS-2 (−)	27B					27B					27B				27B	
GROUND	28A					28A					28A				28A	GROUND
GROUND	28B					28B					28B				28B	
	29A					29A					29A				29A	
	29B					29B					29B				29B	
GROUND	30A					30A					30A				30A	
GROUND	30B					30B					30B				30B	
	31A					31A					31A				31A	
GROUND	31B					31B					31B				31B	
GROUND	32A					32A					32A				32A	
	32B					32B					32B				32B	GROUND
	33A					33A					33A				33A	GROUND
GROUND	33B					33B					33B				33B	
GROUND	34A					34A					34A				34A	
	34B					34B					34B				34B	
	35A					35A					35A				35A	
GROUND	35B					35B					35B				35B	
GROUND	36A					36A					36A				36A	
	36B					36B					36B				36B	
	37A					37A					37A				37A	
GROUND	37B					37B					37B				37B	
GROUND	38A					38A					38A				38A	GROUND
	38B					38B					38B				38B	GROUND
	39A					39A					39A				39A	
GROUND	39B					39B					39B				39B	
GROUND	40A					40A					40A				40A	GROUND
	40B					40B					40B				40B	GROUND
	41A					41A					41A				41A	
GROUND	41B					41B					41B				41B	
GROUND	42A					42A					42A				42A	GROUND
	42B					42B					42B				42B	GROUND
	43A					43A					43A				43A	
GROUND	43B					43B					43B				43B	
GROUND	44A					44A					44A				44A	GROUND
	44B					44B					44B				44B	GROUND
	45A					45A					45A				45A	
GROUND	45B					45B					45B				45B	
GROUND	46A					46A					46A				46A	GROUND
	46B					46B					46B				46B	GROUND
	47A					47A					47A				47A	
GROUND	47B					47B					47B				47B	
GROUND	48A					48A					48A				48A	GROUND
	48B					48B					48B				48B	GROUND
	49A					49A					49A				49A	
GROUND	49B					49B					49B				49B	
GROUND	50A					50A					50A				50A	GROUND
	50B	T				50B					50B				50B	GROUND

NOTES:
CARD SLOT 0 FOR IEEE INTERFACE ONLY.

THIS DRAWING IS OUR PROPERTY.
IT IS NOT TO BE COPIED OR USED
WITHOUT THE WRITTEN CONSENT OF:
WANDEL & GOLTERMANN, INC.

REV	ECN-NO	DATE	NAME

	DATE	NAME
DRAWN	11DEC87	R STUCH
CHKD	5Apr-88	E Maus
APPRVD		

REPLACES:
REPLCD BY 9537-7508.02 REV 1

REV	ECN-NO	DATE	NAME
1	NEW		

UTI-1 MOTHER BOARD
(ST1 CONNECTOR ROW)

SERIES A...C

9537-7508.01/B

PG 2 OF 5

REV	ECN-NO	DATE	NAME
1	NEW		

	DATE	NAME
DRAWN	11DEC87	R STUCH
CHKD	5-Mar-88	E Mayo
APPRVD		

REPLACES:

REPLCD BY 9537-7508.02 REV1

THIS DRAWING IS OUR PROPERTY.
IT IS NOT TO BE COPIED OR USED
WITHOUT THE WRITTEN CONSENT OF:
WANDEL & GOLTERMANN, INC.

J1		J2		J3		J4		J5		J6	
1A	GROUND	1A	GROUND	1A	GROUND	1A	GROUND	1A	GROUND	1A	GROUND
1B	GROUND	1B	GROUND	1B	GROUND	1B	GROUND	1B	GROUND	1B	GROUND
2A	GROUND	2A	GROUND	2A	GROUND	2A	GROUND	2A	GROUND	2A	GROUND
2B		2B		2B		2B		2B		2B	GROUND
3A		3A		3A		3A		3A		3A	
3B	GROUND	3B	GROUND	3B	GROUND	3B	GROUND	3B	GROUND	3B	GROUND
4A	GROUND	4A	GROUND	4A	GROUND	4A	GROUND	4A	GROUND	4A	GROUND
4B		4B		4B		4B		4B		4B	
5A		5A		5A		5A		5A		5A	
5B	GROUND	5B	GROUND	5B	GROUND	5B	GROUND	5B	GROUND	5B	GROUND
6A	GROUND	6A	GROUND	6A	GROUND	6A	GROUND	6A	GROUND	6A	GROUND
6B		6B		6B		6B		6B		6B	
7A		7A		7A		7A		7A		7A	
7B	GROUND	7B	GROUND	7B	GROUND	7B	GROUND	7B	GROUND	7B	GROUND
8A	GROUND	8A	GROUND	8A	GROUND	8A	GROUND	8A	GROUND	8A	GROUND
8B		8B		8B		8B		8B		8B	
9A		9A		9A		9A		9A		9A	
9B	GROUND	9B	GROUND	9B	GROUND	9B	GROUND	9B	GROUND	9B	GROUND
10A	GROUND	10A	GROUND	10A	GROUND	10A	GROUND	10A	GROUND	10A	GROUND
10B		10B		10B		10B		10B		10B	
11A		11A		11A		11A		11A		11A	
11B	GROUND	11B	GROUND	11B	GROUND	11B	GROUND	11B	GROUND	11B	GROUND
12A	GROUND	12A	GROUND	12A	GROUND	12A	GROUND	12A	GROUND	12A	GROUND
12B		12B		12B		12B		12B		12B	
13A		13A		13A		13A		13A		13A	
13B	GROUND	13B	GROUND	13B	GROUND	13B	GROUND	13B	GROUND	13B	GROUND
14A	GROUND	14A	GROUND	14A	GROUND	14A	GROUND	14A	GROUND	14A	GROUND
14B		14B		14B		14B		14B		14B	
15A	COAXIAL MONITOR SIGNAL-1	15A		15A		15A		15A		15A	
15B	COAXIAL MONITOR SIGNAL-2	15B		15B		15B		15B		15B	
16A	GROUND	16A		16A		16A		16A		16A	
16B	GROUND	16B		16B		16B		16B		16B	
17A	ANALOG BUS-1 (DMM+)	17A		17A		17A		17A		17A	
17B	ANALOG BUS-5 (T)	17B		17B		17B		17B		17B	
18A	ANALOG BUS-1 (DMM-)	18A		18A		18A		18A		18A	
18B	ANALOG BUS-5 (R)	18B		18B		18B		18B		18B	
19A	ANALOG BUS-1 (S) GND	19A		19A		19A		19A		19A	
19B	ANALOG BUS-5 (S) GND	19B		19B		19B		19B		19B	ANALOG BUS-1 (S) GND
20A	ANALOG BUS-2 (TRANSMIT-T)	20A		20A		20A		20A		20A	ANALOG BUS-5 (S) GND
20B	ANALOG BUS-6 (ACTIVATION-T)	20B		20B		20B		20B		20B	
21A	ANALOG BUS-2 (TRANSMIT-R)	21A		21A		21A		21A		21A	
21B	ANALOG BUS-6 (ACTIVATION-R)	21B		21B		21B		21B		21B	
22A	ANALOG BUS-2 (S) GND	22A		22A		22A		22A		22A	
22B	ANALOG BUS-6 (S) GND	22B		22B		22B		22B		22B	
23A	ANALOG BUS-3 (RECIEVE-T)	23A		23A		23A		23A		23A	
23B	ANALOG BUS-7 (T)	23B		23B		23B		23B		23B	
24A	ANALOG BUS-3 (RECIEVE-R)	24A		24A		24A		24A		24A	
24B	ANALOG BUS-7 (R)	24B		24B		24B		24B		24B	
25A	ANALOG BUS-3 (S) GND	25A		25A		25A		25A		25A	
25B	ANALOG BUS-7 (S) GND	25B		25B		25B		25B		25B	
26A	ANALOG BUS-4 (T)	26A		26A		26A		26A		26A	
26B	ANALOG BUS-8 (T)	26B		26B		26B		26B		26B	
27A	ANALOG BUS-4 (R)	27A		27A		27A		27A		27A	
27B	ANALOG BUS-8 (R)	27B		27B		27B		27B		27B	
28A	ANALOG BUS-4 (S)	28A		28A		28A		28A		28A	
28B	ANALOG BUS-8 (S)	28B		28B		28B		28B		28B	
29A		29A		29A		29A		29A		29A	
29B		29B		29B		29B		29B		29B	
30A		30A		30A		30A		30A		30A	
30B		30B		30B		30B		30B		30B	
31A		31A		31A		31A		31A		31A	
31B		31B		31B		31B		31B		31B	
32A		32A		32A		32A		32A		32A	
32B		32B		32B		32B		32B		32B	
33A		33A		33A		33A		33A		33A	
33B		33B		33B		33B		33B		33B	
34A		34A		34A		34A		34A		34A	CARD SELECT 15
34B		34B		34B		34B		34B		34B	CARD SELECT 7
35A		35A		35A		35A		35A		35A	CARD SELECT 14
35B		35B		35B		35B		35B		35B	CARD SELECT 6
36A		36A		36A		36A		36A		36A	CARD SELECT 13
36B		36B		36B		36B		36B		36B	CARD SELECT 5
37A		37A		37A		37A		37A		37A	CARD SELECT 12
37B	CARD SELECT 11	37B		37B		37B		37B		37B	CARD SELECT 4
38A	LOOP BACK SIG-1	38A		38A		38A		38A		38A	CARD SELECT 11
38B	LOOP BACK SIG-2	38B		38B		38B		38B		38B	CS-3
39A	CLOCK-2	39A		39A		39A		39A		39A	CS-10
39B	CLOCK-4	39B		39B		39B		39B		39B	CS-2
40A	CLOCK-1	40A		40A		40A		40A		40A	CS-9
40B	CLOCK-3	40B		40B		40B		40B		40B	CS-1
41A	LISTEN 2**3/DIO3	41A		41A		41A		41A		41A	CS-8
41B	LISTEN 2**3/DIO7	41B		41B		41B		41B		41B	LISTEN 2**3/DIO3
42A	TALK 2**2/DIO2	42A		42A		42A		42A		42A	LISTEN 2**3/DIO7
42B	LISTEN 2**2/DIO6	42B		42B		42B		42B		42B	TALK 2**2/DIO2
43A	TALK 2**1/DIO1	43A		43A		43A		43A		43A	LISTEN 2**2/DIO6
43B	LISTEN 2**1/DIO5	43B		43B		43B		43B		43B	TALK 2**1/DIO1
44A	TALK 2**0/DIO0	44A		44A		44A		44A		44A	LISTEN 2**1/DIO5
44B	LISTEN 2**0/DIO0	44B		44B		44B		44B		44B	TALK 2**0/DIO0
45A	TALK-LISTEN / EOI	45A		45A		45A		45A		45A	LISTEN 2**0/DIO0
45B	REMOTE / LOCAL	45B		45B		45B		45B		45B	TALK-LISTEN / EOI
46A	ATN	46A		46A		46A		46A		46A	REMOTE / LOCAL
46B	MBUS CLEAR	46B		46B		46B		46B		46B	ATN
47A	POSITION 2**3	47A		47A		47A		47A		47A	MBUS CLEAR
47B	TRIGGER-2	47B		47B		47B		47B		47B	POSITION 2**3
48A	POSITION 2**2 / NDAC	48A		48A		48A		48A		48A	TRIGGER-2
48B	TRIGGER-1	48B		48B		48B		48B		48B	POSITION 2**2 / NDAC
49A	POSITION 2**1 / NRFD	49A		49A		49A		49A		49A	TRIGGER-1
49B	RESET	49B		49B		49B		49B		49B	POSITION 2**1 / NRFD
50A	POSITION 2**0 / DAV	50A		50A		50A		50A		50A	RESET
50B	CARD SELECT	50B		50B		50B		50B		50B	POSITION 2**0 / DAV
		CS15		CS14		CS13		CS12		CS11	CS10
											CS9
											CS8
											CS7
											CS6
											CS5
											CS4
											CS3
											CS2
											CS1

UTI-1 MOTHER BOARD (ST2 CONNECTOR ROW)	SERIES A...C		
	9537-7508.01/B	PG 3 OF 5	

Component side	A	B	Non-Component Side
A/V-2 [2]	1		A/V-2 [2]
A/V-3 [2]	2		
A/V-1A (+75 Volts) [2]	3		AV-1Q (+ 75 Volts Return) [2]
A/V-41 (Ringing AC H) [2]	4		AV-42 (Ringing AC L) [2]
A/V-51 (Ringing DC +) [2]	5		AV-52 (Ringing DC -) [2]
V1 (+)	6		V1 (-)
V2 (+)	7		V2 (-)
V3 (+)	8		V3 (-)
V4 (+)	9		V4 (-)
V5 (+)	10		V5 (-)
V6 (+)	11		V6 (-)
V7 (+)	12		V7 (-)
V8 (+)	13		V8 (-)
+ 15 Volts	14		- 15 Volts
+ 5 Volts	15		+ 5 Volts
A/C-2 (Zero xing +ve in)	16		A/C-3 (Zero xing -ve in)
A/C-4 (Zero xing low level in)	17		A/C-5 (Zero xing out)
A/C-1 (Interlock)	18		A/C-6 (Summing Amplifier Out)
Ground	19		Ground
Ground	20		Interconnect Bus-1
Interconnect Bus-2	21		Ground
Ground	22		Interconnect Bus-1 Return
Interconnect Bus-2 Return	23		Ground
Ground	24		Aux DMM Bus-1 (+)
Aux DMM Bus-2 (+)	25		Ground

Component side	A	B	Non-Component Side
Ground	26		Aux DMM Bus-1 (-)
Aux DMM Bus-2 (-)	27		Ground
Ground	28		
	29		Ground
Ground	30		
	31		Ground
Ground	32		
	33		Ground
Ground	34		
	35		Ground
Ground	36		
	37		Ground
Ground	38		
	39		Ground
Ground	40		
	41		Ground
Ground	42		
	43		Ground
Ground	44		
	45		Ground
Ground	46		
	47		Ground
Ground	48		
	49		Ground
Ground	50		

	NAME	DATE	ECN-NO	REV

THIS DRAWING IS OUR PROPERTY.
IT IS NOT TO BE COPIED OR USED
WITHOUT THE WRITTEN CONSENT OF:
WANDEL & GOLTERMANN, INC.

	NAME	DATE
DRAWN	MEH	25 AUG 87
CHKD		5 Apr 91
APPRVD		
REPLACES		
REPLCD BY 9537-7508.02 rev1		

REV	ECN-NO	DATE	NAME
1	NEW		

	NAME	DATE

UTI-1 MOTHER BOARD
CONNECTOR BU1 [1]

SERIES A...C

9537-7508.01/B

PG 4
OF 5

Component side	A	B	Non-Component Side
	1		Ground
Ground	2		
	3		Ground
Ground	4		
	5		Ground
Ground	6		
	7		Ground
Ground	8		
	9		Ground
Ground	10		
	11		Ground
Ground	12		
	13		Ground
Ground	14		
Coaxial Monitor Signal-1	15		Coaxial Monitor Signal-2
Ground	16		Ground
Analog Bus-1 (DMM +)	17		Analog Bus-5 (T)
Analog Bus-1 (DMM -)	18		Analog Bus-5 (R)
Analog Bus-1 (S) Ground	19		Analog Bus-5 (S), Ground
Analog Bus-2 (Transmit-T)	20		Analog Bus-6 (Activation - T)
Analog Bus-2 (Transmit-R)	21		Analog Bus-6 (Activation - R)
Analog Bus-2 (S), Ground	22		Analog Bus-6 (S), Ground
Analog Bus-3 (Receive-T)	23		Analog Bus-7 (T)
Analog Bus-3 (Receive-R)	24		Analog Bus-7 (R)
Analog Bus-3 (S), Ground	25		Analog Bus-7 (S), Ground

Component side	A	B	Non-Component Side
Analog Bus-4 (T)	26		Analog Bus-8 (T)
Analog Bus-4 (R)	27		Analog Bus-8 (R)
Analog Bus-4 (S)	28		Analog Bus-8 (S)
	29		
	30		
	31		
	32		
	33		$\overline{\text{Card Select 15}}$ [3]
$\overline{\text{Card Select 7}}$ [3]	34		$\overline{\text{Card Select 14}}$ [3]
$\overline{\text{Card Select 6}}$ [3]	35		$\overline{\text{Card Select 13}}$ [3]
$\overline{\text{Card Select 5}}$ [3]	36		$\overline{\text{Card Select 12}}$ [3]
$\overline{\text{Card Select 4}}$, G-CH1 [3]	37		$\overline{\text{Card Select 11}}$ [3]
$\overline{\text{CS-3}}$, Loop Back Sig-1 [3]	38		$\overline{\text{CS 10}}$, Loop Back Sig-2 [3]
$\overline{\text{Card Select 2}}$, Clock-2 [3]	39		$\overline{\text{Card Select 9}}$, Clock-4 [3]
$\overline{\text{Card Select 1}}$, Clock-1 [3]	40		$\overline{\text{Card Select 8}}$, Clock-3 [3]
Talk 2**3 / DIO3	41		Listen 2**3 / DIO7
Talk 2**2 / DIO2	42		Listen 2**2 / DIO6
Talk 2**1 / DIO1	43		Listen 2**1 / DIO5
Talk 2**0 / DIO0	44		Listen 2**0 / DIO0
$\overline{\text{Talk}}$ -Listen / EOI	45		Remote / $\overline{\text{Local}}$
$\overline{\text{ATN}}$	46		$\overline{\text{MBUS Clear}}$
Position 2**3 /	47		$\overline{\text{Trigger-2}}$
Position 2**2 / $\overline{\text{NDAC}}$	48		$\overline{\text{Trigger-1}}$
Position 2**1 / $\overline{\text{NRFD}}$	49		$\overline{\text{Reset}}$
Position 2**0 / $\overline{\text{DAV}}$	50		$\overline{\text{Card Select}}$

THIS DRAWING IS OUR PROPERTY.
IT IS NOT TO BE COPIED OR USED
WITHOUT THE WRITTEN CONSENT OF:
WANDEL & GOLTERMANN, INC.

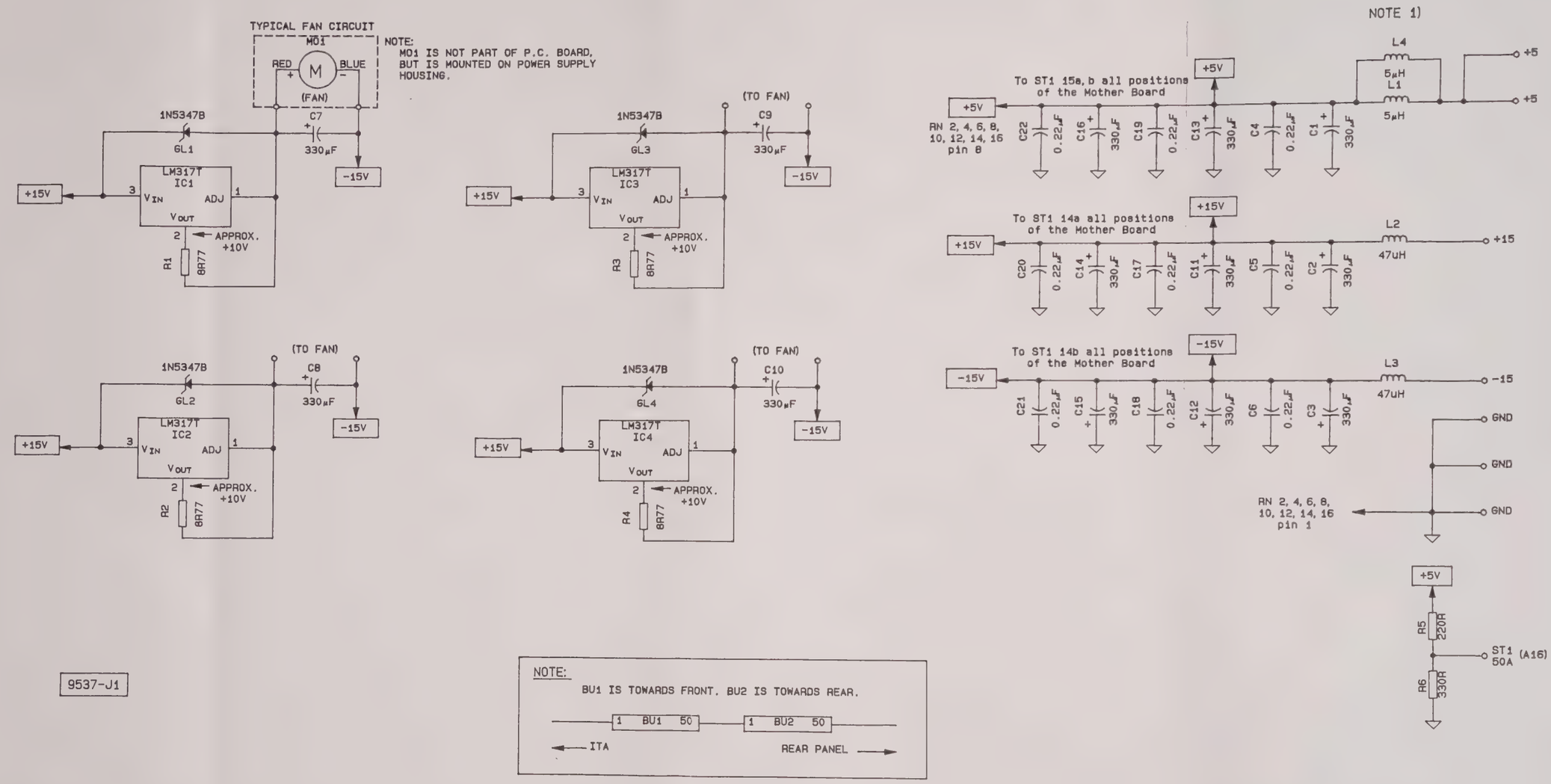
	NAME	DATE	ECN-NO	REV
DRAWN	WEH	25 AUG 87	NEW	1
CHKD				
APPRVD				
REPLACES				
REPLCD BY 9537-7508.02 rev1				

UTI-1 MOTHER BOARD
CONNECTOR BU2 [1]

SERIES A...C

9537-7508.01/B

PG 5 OF 5



UTI-1 MOTHER BOARD ELECTRONICS

NOTE 1) L4 IS INSTALLES IN SERIES E...ON ONLY

REV	ECN-NO	DATE	NAME
1	88-038	08MAR88	L M G
2	88-072	12MAY88	L M G
3	88-144	13DEC88	DHB
4	89-019	07MAR89	M R M

	DATE	NAME
DRAWN	13 JAN 88	SCHILLER
CHKD	[illegible]	[illegible]
APPRVD		
REPLACES: 9537-7508.01 REV1		
REPLCD BY		

THIS DRAWING IS OUR PROPERTY. IT IS NOT TO BE COPIED OR USED WITHOUT THE WRITTEN CONSENT OF:

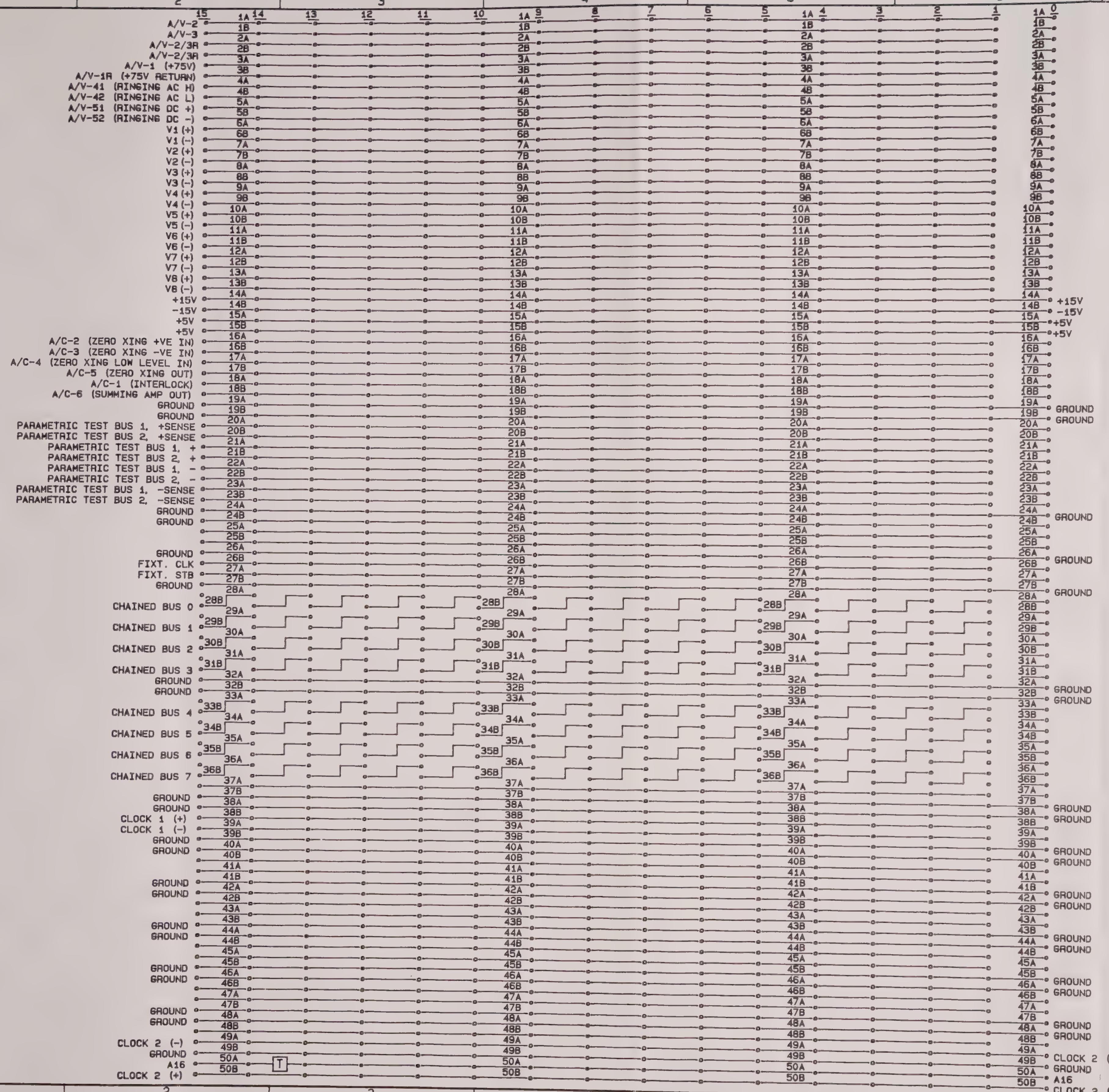
WANDEL & GOLTERMANN, INC.

UTI-1 MOTHER BOARD

SERIES D...

9537-7508.02/B

PG 1 OF 7



REV	ECN-NO	DATE	NAME
1	88-038	08MAR88	L M G
2	88-072	12MAY88	L M G
3	88-144	13DEC88	DHB
4	89-019	07MAR88	MRM

	DATE	NAME
DRAWN	11DEC87	R STUCH
CHKD		
APPRVD		
REPLACES: 9537-7508.01 REV1		
REPLCD BY		

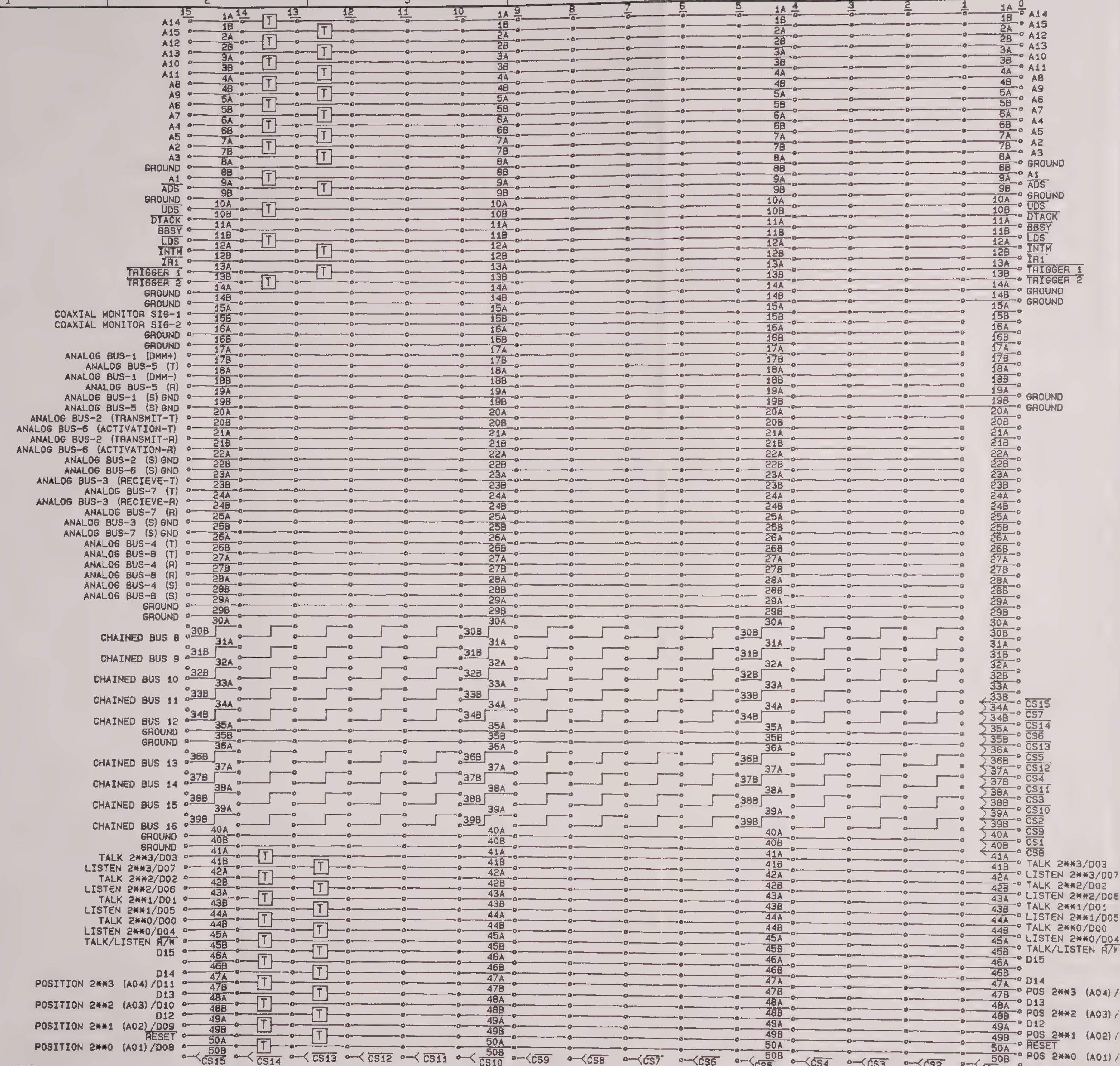
THIS DRAWING IS OUR PROPERTY.
IT IS NOT TO BE COPIED OR USED
WITHOUT THE WRITTEN CONSENT OF:
WANDEL & GOLTERMANN, INC.

NOTES:
CARD SLOT 0 FOR IEEE INTERFACE ONLY.

UTI-1 MOTHER BOARD
(ST1 CONNECTOR ROW)

SERIES D...

9537-7508.03/B



REV	ECN-NO	DATE	NAME
1	88-038	08MAR88	L M G
2	88-072	12MAY88	L M G
3	88-144	13DEC88	DHB
4	89-019	07MAR89	MRM

	DATE	NAME
DRAWN	11DEC87	R STUCH
CHKD		
APPRVD		

REPLACES: 9537-7508.01 REV1

REPLCD BY

THIS DRAWING IS OUR PROPERTY. IT IS NOT TO BE COPIED OR USED WITHOUT THE WRITTEN CONSENT OF:

WANDEL & GOLTERMANN, INC.

WG

UTI-1 MOTHER BOARD
(ST2 CONNECTOR ROW)

SERIES D...

9537-7508.03/B

Component side	A	BU1	B	Non-Component Side
A/V-2 (+150V) 1)		1		A/V-3 (-150V) 1)
A/V-2/3R (±150V RETURN) 1)		2		A/V-2/3R (±150V RETURN) 1)
A/V-1 (+75V) 1)		3		A/V-1R (+75V RETURN) 1)
A/V-41 (Ringing AC-H) 1)		4		A/V-42 (Ringing AC-L) 1)
A/V-51 (Ringing DC+) 1)		5		A/V-52 (Ringing DC-) 1)
V1 (+) 2)		6		V1 (-) 2)
V2 (+) 2)		7		V2 (-) 2)
V3 (+) 2)		8		V3 (-) 2)
V4 (+) 2)		9		V4 (-) 2)
V5 (+) 2)		10		V5 (-) 2)
V6 (+) 2)		11		V6 (-) 2)
V7 (+) 2)		12		V7 (-) 2)
V8 (+) 2)		13		V8 (-) 2)
+ 15 Volts 3)		14		- 15 Volts 3)
+ 5 Volts 3)		15		+ 5 Volts 3)
A/C-2 (Zero Xing +Ve In) 4) 17)		16		A/C-3 (Zero Xing -Ve In) 4) 17)
A/C-4 (Zero Xing Low Level In) 4) 17)		17		A/C-5 (Zero Xing Out) 4) 17)
A/C-1 (Interlock) 4) 17)		18		A/C-6 (Summing Amp Out) 4) 17)
Ground		19		Ground
Parametric Test Bus 1, +Sense 5)		20		Parametric Test Bus 2, +Sense 5)
Parametric Test Bus 1, + 5)		21		Parametric Test Bus 2, + 5)
Parametric Test Bus 1, - 5)		22		Parametric Test Bus 2, - 5)
Parametric Test Bus 1, -Sense 5)		23		Parametric Test Bus 2, -Sense 5)
Ground		24		Ground 6)
7) 17)		25		7) 17)

Component side	A	BU1	B	Non-Component Side
Ground		26		Fixture Clock 8)
Fixture Strobe 8)		27		Ground
Daisy Chained Bus 0 9)		28		Daisy Chained Bus 0 9)
Daisy Chained Bus 1 9)		29		Daisy Chained Bus 1 9)
Daisy Chained Bus 2 9)		30		Daisy Chained Bus 2 9)
Daisy Chained Bus 3 9)		31		Daisy Chained Bus 3 9)
Ground		32		Ground
Daisy Chained Bus 4 9)		33		Daisy Chained Bus 4 9)
Daisy Chained Bus 5 9)		34		Daisy Chained Bus 5 9)
Daisy Chained Bus 6 9)		35		Daisy Chained Bus 6 9)
Daisy Chained Bus 7 9)		36		Daisy Chained Bus 7 9)
7)		37		Ground
Ground		38		CLK 1+ 10) CLK 1
CLK 1- 10) CLK 2		39		Ground
Ground		40		7) 17)
7) 17)		41		Ground
Ground		42		7) 17)
DEL CLK 7) 18)		43		Ground
Ground		44		EXT STR 7) 18)
DEL STB 7) 18)		45		Ground
Ground		46		SHIFT CLK 7) 18)
$\overline{SF}$ 7) 18)		47		Ground
Ground		48		7)
CLK 2- 11)		49		Ground
A16 (R5, R6) 12)		50		CLK 2+ 11)

IMPORTANT:

THIS INFORMATION IS APPLICABLE TO REV.4 & UP
MOTHERBOARDS ONLY (UTI-1 SERIES D & UP)

REV	ECN-NO	DATE	NAME
1	88-038	08MAR88	L M G
2	88-072	12MAY88	L M G
3	88-144	13DEC88	DHB
4	89-019	06MAR89	M R M

	DATE	NAME
DRAWN	13 JAN 88	SCHILLER
CHKD		
APPRVD		

REPLACES: 9537-7508.01 REV1
REPLCD BY

THIS DRAWING IS OUR PROPERTY.
IT IS NOT TO BE COPIED OR USED
WITHOUT THE WRITTEN CONSENT OF:
WANDEL & GOLTERMANN, INC.

UTI-1 MOTHER BOARD

SERIES D...

9537-7508.02/B

Component side		A BU2 B	Non-Component Side	
A14 (RN14, PIN 7)	12)	1	A15 (RN10, PIN 7)	12)
A12 (RN14, PIN 6)	12)	2	A13 (RN10, PIN 6)	12)
A10 (RN14, PIN 5)	12)	3	A11 (RN10, PIN 5)	12)
A8 (RN14, PIN 4)	12)	4	A9 (RN10, PIN 4)	12)
A6 (RN14, PIN 3)	12)	5	A7 (RN10, PIN 3)	12)
A4 (RN14, PIN 2)	12)	6	A5 (RN10, PIN 2)	12)
A2 (RN16, PIN 3)	12)	7	A3 (RN16, PIN 4)	12)
Ground		8	A1 (RN16, PIN 2)	12)
$\overline{AS}$ (RN12, PIN 7)	12)	9	Ground	
$\overline{UDS}$ (RN12, PIN 6)	12)	10	$\overline{DTACK}$	12)
$\overline{BBSY}$	12)	11	$\overline{LDS}$ (RN12, PIN 5)	12)
$\overline{INTM}$ (RN12, PIN 4)	12)	12	$\overline{IR}$	12)
$\overline{TRIGGER\ 1}$ (RN12, PIN 3)	12)	13	$\overline{TRIGGER\ 2}$ (RN12, PIN 2)	12) 15)
Ground		14	Ground	
Coaxial Monitor Signal-1	13)	15	Coaxial Monitor Signal-2	13)
Ground		16	Ground	
Analog Bus-1 (DMM +)	14)	17	Analog Bus-5 (T)	14)
Analog Bus-1 (DMM -)	14)	18	Analog Bus-5 (R)	14)
Analog Bus-1 (S) Ground	14)	19	Analog Bus-5 (S), Ground	14)
Analog Bus-2 (Transmit-T)	14)	20	Analog Bus-6 (Activation - T)	14)
Analog Bus-2 (Transmit-R)	14)	21	Analog Bus-6 (Activation - R)	14)
Analog Bus-2 (S), Ground	14)	22	Analog Bus-6 (S), Ground	14)
Analog Bus-3 (Receive-T)	14)	23	Analog Bus-7 (T)	14)
Analog Bus-3 (Receive-R)	14)	24	Analog Bus-7 (R)	14)
Analog Bus-3 (S), Ground	14)	25	Analog Bus-7 (S), Ground	14)

Component side		A BU2 B	Non-Component Side	
Analog Bus-4 (T)	14)	26	Analog Bus-8 (T)	14)
Analog Bus-4 (R)	14)	27	Analog Bus-8 (R)	14)
Analog Bus-4 (S)	14)	28	Analog Bus-8 (S)	14)
GND	6)	29	GND	6)
Daisy Chained Bus 8	9)	30	Daisy Chained Bus 8	9)
Daisy Chained Bus 9	9)	31	Daisy Chained Bus 9	9)
Daisy Chained Bus 10	9)	32	Daisy Chained Bus 10	9)
Daisy Chained Bus 11	9)	33	$\overline{Card\ Select\ 15}$ Daisy Chained Bus 11	16) 9)
$\overline{Card\ Select\ 7}$ Daisy Chained Bus 12	16) 9)	34	$\overline{Card\ Select\ 14}$ Daisy Chained Bus 12	16) 9)
$\overline{Card\ Select\ 6}$ GND	16) 6)	35	$\overline{Card\ Select\ 13}$ GND	16) 6)
$\overline{Card\ Select\ 5}$ Daisy Chained Bus 13	16) 9)	36	$\overline{Card\ Select\ 12}$ Daisy Chained Bus 13	16) 9)
$\overline{Card\ Select\ 4}$ Daisy Chained Bus 14	16) 9)	37	$\overline{Card\ Select\ 11}$ Daisy Chained Bus 14	16) 9)
$\overline{Card\ Select\ 3}$ Daisy Chained Bus 15	16) 9)	38	$\overline{Card\ Select\ 10}$ Daisy Chained Bus 15	16) 9)
$\overline{Card\ Select\ 2}$ Daisy Chained Bus 16	16) 9)	39	$\overline{Card\ Select\ 9}$ Daisy Chained Bus 16	16) 9)
$\overline{Card\ Select\ 1}$ Ground	16) 6)	40	$\overline{Card\ Select\ 8}$ Ground	16) 6)
Talk 2^3 D_{03} (RN6, PIN 5)	15) 12)	41	LISTEN 2^3 D_{07} (RN8, PIN 5)	15) 12)
Talk 2^2 D_{02} (RN6, PIN 4)	15) 12)	42	LISTEN 2^2 D_{06} (RN8, PIN 4)	15) 12)
Talk 2^1 D_{01} (RN6, PIN 3)	15) 12)	43	LISTEN 2^1 D_{05} (RN8, PIN 3)	15) 12)
Talk 2^0 D_{00} (RN6, PIN 2)	15) 12)	44	LISTEN 2^0 D_{04} (RN8, PIN 2)	15) 12)
$\overline{Talk}$ / Listen R / $\overline{W}$ (RN8, PIN 7)	15) 12)	45	D_{15} (RN4, PIN 7)	15)
(RN8, PIN 6)	15) 6)	46	D_{14} (RN4, PIN 6)	15)
Position 2^3 D_{11} (RN8, PIN 5)	15) 12)	47	D_{13} (RN4, PIN 5)	15)
Position 2^2 D_{10} (RN8, PIN 4)	15) 12)	48	D_{12} (RN4, PIN 4)	15)
Position 2^1 D_{09} (RN8, PIN 3)	15) 12)	49	$\overline{RESET}$ (RN4, PIN 3)	15) 12)
Position 2^0 D_{08} (RN8, PIN 2)	15) 12)	50	$\overline{Card\ Select}$	16)

IMPORTANT:

THIS INFORMATION IS APPLICABLE TO REV.4 & UP
MOTHERBOARDS ONLY (UTI-1 SERIES D & UP)

REV	ECN-NO	DATE	NAME

THIS DRAWING IS OUR PROPERTY.
IT IS NOT TO BE COPIED OR USED
WITHOUT THE WRITTEN CONSENT OF:
WANDEL & GOLTERMANN, INC.

	DATE	NAME
DRAWN	13 JAN 88	SCHILLER
CHKD		
APPRVD		
REPLACES: 9537-7508.01 REV1		
REPLCD BY		

REV	ECN-NO	DATE	NAME
1	88-038	08MAR88	L M G
2	88-072	12MAY88	L M G
3	88-144	13DEC88	DHB
4	89-019	07MAR89	M R M

WG	UTI-1 MOTHER BOARD	SERIES D...	
		9537-7508.02/B	PG 5 OF 7

Endnotes to Wiring Sheets of UTI-1 Motherboard

Note: Unless otherwise stated, all lines connect to the same numbered pins on slots 1 through 15. Ground lines connect between all slots except where noted in endnote 6).

1) The pairs of lines BU1 1A/2A and BU1 1B/2B are designed to handle up to 150 volts from external sources. BU1 pins 2A and 2B are connected together for all the 15 slots.

   If the W&G Analog Module (BN9537/00.03 is installed in the UTI-1, these lines may be used to connect voltages from external power supplies to the motherboard. Jumpers on the Analog Module will have to be installed to connect these voltages through to the motherboard. These jumpers are not installed at the factory. See the description of the Analog Module for details.

   The factory markets a Ringing Generator that interfaces to the UTI-1 through the W&G Analog Module (9537/00.03). When the Ringing Generator and Analog Module with the appropriate jumpers as mentioned in the above paragraph are installed, these lines are dedicated to the voltages produced by the Ringing Generator (Ringing AC, Ringing DC) and the external high voltage power supplies (75 Volts, +150 Volts, -150 Volts) needed to provide the ringing functions.

   An external 15 Volt source can be connected through these lines for use on UTI-1 boards featuring "pin electronics" hybrids.

2) If the W&G Analog Module (9537/00.03) is installed in the UTI-1, these lines may be used to connect voltages from up to eight independent external power supplies from the rear panel to the motherboard. The voltage lines are provided in pairs to provide floating voltages. Jumpers on the Analog Module will have to be installed to connect these voltages through to the motherboard. These jumpers are not installed at the factory. See description of the Analog Module for details.

   Relays on the Analog Module control the connection of these voltages. The voltage pairs designated V1 and V4 have independent relays. The connection of V5 and V6 are controlled together, and the connection of V7 and V8 are controlled together.

   If the power supplies provide sense lines, provisions must be made to connect them to the voltage lines on the Interchangeable Test Adapter (ITA). If these connections are made on the personality board, care must be taken to prevent the output voltages from rising when the ITA is removed (breaking the connection between the voltage and sense lines). This may be accomplished, for example, by installation of low value resistors installed between voltage and sense lines near the power supplies.

3) These lines connect to all slots, 0 through 15, and are hardwired to the internal 175 watt regulated power supply in the UTI-1. See Section 2 of this manual for the specifications of the individual voltages.

4) If the Ringing Generator is connected through the W&G Analog Module (BN9537/00.03), these lines provide certain control functions for the Ringing Generator. One of these, the Interlock (BU1 pin 18A) must be connected to ground to allow the Ringing Generator to output voltages. Jumpers on the Analog Module will have to be installed to connect these lines through the motherboard. These jumpers are not installed at the factory. See the description of the Analog Module for more details.

5) When the W&G Standard Latch Module (9537/00.24) is installed, these pins are used by the two Parametric Test Busses for pin electronic tests. These busses connect voltage and current sources from other UTI-1 pc boards to individual pins of the device under test on the personality board. One bus can provide the source voltage or current while the other can be used to sense the effect on another test pin.

6) These grounds do not extend to slot 0.

7) UNBALANCED BUS LINES: These lines may be used for any unbalanced digital or analog signal which is less than 35 volts. These lines are shielded on both sides and above and below. They extend from slot 1 through slot 15.

8) These lines connect to the W&G Digital Interface board (if installed). Jumpers must be installed on the Digital Interface if these lines are to be used as Fixture Clock and Strobe. In a PCM application, these lines would be needed to provide clock and strobe to the system if they originate on a board in the UTI-1. A foreseeable application would be the inclusion of a synthesizer board to provide the clock and strobe.

9) The daisy chained lines 0 to 16 connect between adjacent pairs of cards in slots 1 through 15. A connection at an "A" pin will connect to the adjacent slot at a "B" pin. This arrangement allows signals to be used by a limited number of cards, and the same lines can be used for other signals between different cards. For example, a signal generated on a card in slot 3 can be put onto Daisy Chain Bus 5 by connecting to BU1 pin 31A. This signal can be picked up by the card in slot 4 by connecting to BU1 pin 31B. The signal will only be passed to the card in slot 5 if the card in slot 4 connects this signal to BU1 pin 31A.

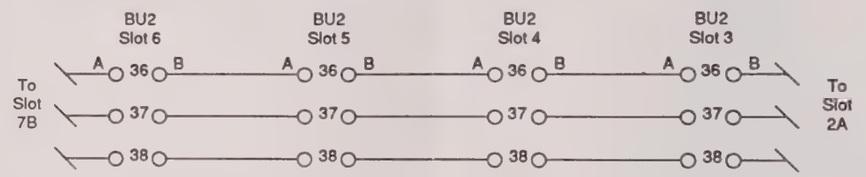


Figure 1 Daisy Chained Bus Wiring Example

   In ISDN testing applications, these lines are dedicated for digital transmit signals originating in the Pattern Generators.

10) CLK1- and CLK1+ are adjacent bus lines running between all the slots except slot 0. These clock lines may be used as a differential pair and are primarily intended to synchronize clocks between microprocessors installed on the various UTI-1 boards.

    In ISDN testing applications, these lines are dedicated as individual clock lines which are labelled CLK-1 and CLK-2 and originate in the Pattern Generators.

11) CLK2- and CLK2+ are adjacent bus lines running between all the slots including slot 0. These clock lines may be used as a differential pair and are primarily intended to synchronize clocks to the clock on the controller board.

12) The designations show lines which are used when the Parallel Bus Interface Module is installed in slot 0. These include 16 address lines, 16 bidirectional data lines, an address strobe ($\overline{AS}$), an upper data strobe ($\overline{UDS}$), and a lower data strobe ($\overline{LDS}$) and ($\overline{RESET}$). Additionally, there are three handshaking lines that send information from UTI-1 cards to the system controller. These are bus busy ($\overline{BBSY}$), interrupt request ($\overline{IR}$), and data acknowledge ($\overline{DTACK}$). Two trigger lines, ($\overline{TRIGGER\ 1}$) and ($\overline{TRIGGER\ 2}$), and a module interrupt line ($\overline{INTM}$) are included for those signals originating on the parallel Bus Interface Module.

IMPORTANT:

THIS INFORMATION IS APPLICABLE TO REV.4 & UP
MOTHERBOARDS ONLY (UTI-1 SERIES D & UP)

THIS DRAWING IS OUR PROPERTY.
IT IS NOT TO BE COPIED OR USED
WITHOUT THE WRITTEN CONSENT OF:
WANDEL & GOLTERMANN, INC.

	NAME	DATE
DRAWN	SCHILLEH	13 JAN 88
CHKD		
APPRVD		
REPLACES	9537-7508.01 REV1	
REPLCD BY		

REV	ECN-NO	DATE	NAME
1	88-038	08MAR88	L M G
2	88-072	12MAY88	L M G
3	88-144	13JUE088	UHb
4	89-019	06MAR89	M R M

	NAME
HEV	
ECN-NO	
DATE	
NAME	
REV	
ECN-NO	
DATE	
NAME	

W&G	UTI-1 MOTHER BOARD	SERIES D...	
		9537-7508.02 /B	PG 6 OF 7

The circuitry on each of the other UTI-1 boards must not present more than one standard TTL load. Those lines that pass information to the Parallel Bus Interface Module (the data bus, $\overline{BBSY}$, $\overline{IR}$, and $\overline{DTACK}$) must be able to be tristated on each UTI-1 board using these lines. In addition, driver circuitry on these UTI-1 boards must be able to drive the termination and line impedance (approximately 100 ohms).

Notes in parentheses indicate connections to a resistance package installed on the motherboard containing the line terminations. All the lines except those that pass information only to the controller card are terminated on the motherboard near slot 13. Those lines not terminated on the motherboard will be terminated on the Parallel Bus Interface Module. See Figure 2 for termination details.

Note: $\overline{RESET}$, $\overline{TRIGGER\ 1}$, and $\overline{TRIGGER\ 2}$ are used by both the IEEE Interface Module and the Parallel Bus Interface Module.

13) The Analog Module (9537/00.03) has two 50/75 ohm coaxial connectors on its rear panel that connect to these motherboard lines. Relay contacts are placed on the Analog Board to isolate these lines.

14) These are designed to provide 8 balanced busses for analog signals (up to 620 KHz). Each bus consists of three lines, a ground or shield, a Tip line and a Ring line. The Tip and Ring designations conform to telephone terminology and represent the hot and return lines of a balanced bus. These lines on the motherboard have been specifically designed to minimize cross-talk. They simulate twisted pairs by crossing between layers as they proceed from slot to slot across the motherboard.

15) These designations show lines which are used when the IEEE Interface Module is installed in slot 0. The IEEE Interface Module translates commands from the System Controller to signals that control circuitry on the other UTI-1 boards. The card selects, position lines, and the talk lines are used to write data to a particular card. The card selects, position lines, and listen lines are used to send information from a particular card to the System Controller. These lines are all terminated on the motherboard. Each UTI-1 board that connects to these signals must provide buffering and the ability to tristate the listen lines.

Notes in parentheses indicate connections to a resistance package installed on the motherboard containing the line termination details. All lines except those that pass information only to the controller card are terminated on the motherboard near slot 13. Those lines not terminated on the motherboard will be terminated on the Parallel Bus Interface Module.

Note: $\overline{RESET}$, $\overline{TRIGGER\ 1}$, and $\overline{TRIGGER\ 2}$ may be used by both the IEEE Interface Module and the Parallel Bus Interface Module.

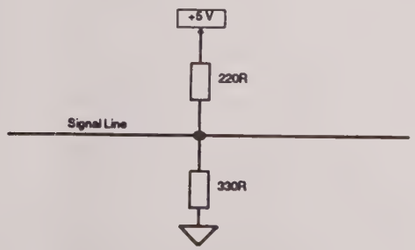


Figure 2 Motherboard Terminations

16) The CARD SELECT LINES allow the controller card in slot 0 to address a particular card in slot 1 through 15. Card Select 1 through Card Select 15 originate at slot 0 (controller card) and connect to BU2 pin 50B of each of the corresponding slots 1 through 15. There is no connection at BU2 pin 50B at slot 0. Circuitry on the controller card in slot 0 allows only one of these lines to go low at a time.

17) In ISDN testing applications, these lines are dedicated to the Record signals for the Pattern Generator/Recorders.

18) In ISDN testing applications, these lines are dedicated to signals necessary for the Pattern Generator/Recorder operation. These signals consist of the Delayed Clock (DEL CK), the Delayed Strobe (DEL STB), External Start (EXT STR), the PCM Shift-in Clock (SHIFT CK), and the Signal Frame ($\overline{SF}$).

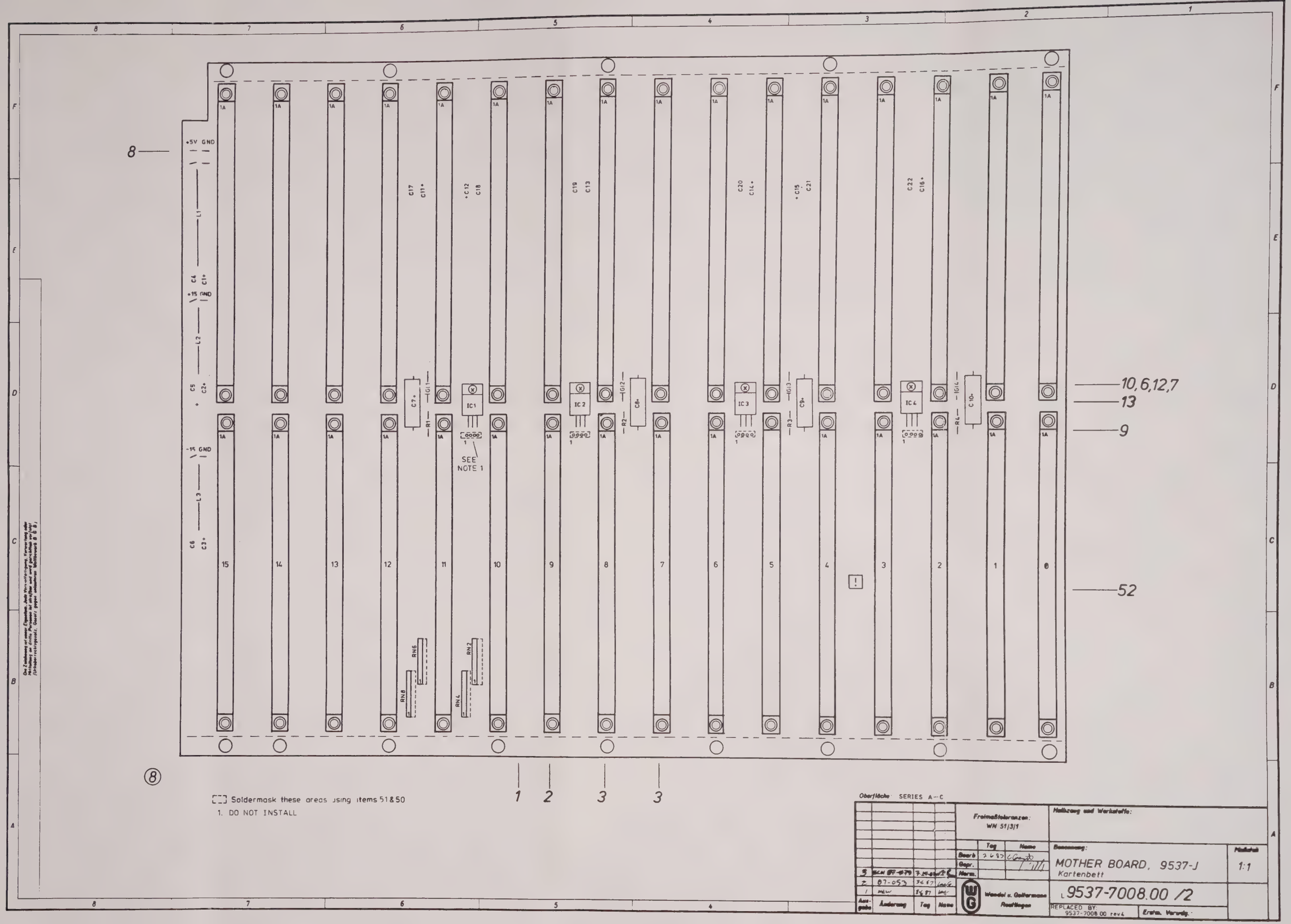
IMPORTANT:

THIS INFORMATION IS APPLICABLE TO REV.4 & UP MOTHERBOARDS ONLY (UTI-1 SERIES D & UP)

REV	ECN-NO	DATE	NAME
1	88-038	08MAR88	
2	88-072	12MAY88	
3	88-144	13DEC88	
4	89-019	06MAR89	

	NAME	DATE
DRAWN	SCHILLER	13 JAN 88
CHKD		10 Feb 89
APPRVD		
REPLACES	9537-7508.01 REV1	
REPLCD BY		

THIS DRAWING IS OUR PROPERTY.
IT IS NOT TO BE COPIED OR USED
WITHOUT THE WRITTEN CONSENT OF:
WANDEL & GOLTERMANN, INC.



Soldermask these areas using items 51 & 50

1. DO NOT INSTALL

Oberfläche: SERIES A–C

Ausgabe	Änderung	Tag	Name
3	ECN 87-079	7.24.87	
2	87-053	3.6.87	
1	NEW	3.6.87	

Freimaßtoleranzen: WN 51/3/1

	Tag	Name
Bearb.	2.6.87	
Gepr.		
Norm.		

Wandel u. Gottermann Reutlingen

Halbzeug und Werkstoffe:

Benennung: MOTHER BOARD, 9537-J Kartenbett

Maßstab 1:1

L 9537-7008.00 /2

REPLACED BY: 9537-7008.00 rev4

Erstm. Verwdg.:

8

GND
GND
GND
L1
+5V
+5V
+5V
L4
*15
GND
L2
C5
C2
-15
GND
L3
C6
C3

C4
C1
C17
C11
C18
C12
C19
C13
C20
C14
C21
C15
C22
C16

IC 1
IC 2
IC 3
IC 4
C7
C8
C9
C10
R1
R2
R3
R4
GI1
GI2
GI3
GI4
R5
R6
RN 16
RN 14
RN 10
RN 12
RN 8
RN 6
RN 4
RN 2

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

10, 6, 12, 7
13
9
52

8

1 2 3 3

Soldermask these areas using items 51 & 50.

Oberfläche: SERIES E...

Freimaßtoleranzen: WN 51/3/1

Halbzeug und Werkstoffe:

					Tag	Name
6	89-016	1-MAR-89	DHB			
5	88-144	22-12-88	DHB	Bearb.	2-6-87	
4	ECN 87-142	10-9-87	P.STICH	Gepr.		
3	ECN 87-079	7-5-87	P.S.	Norm.		
2	87-053	3-6-87	[illegible]			
1	NEW	5-6-87	MG			
Ausgabe	Änderung	Tag	Name			

Wandel u. Goltermann Reutlingen

Benennung: MOTHER BOARD, 9537-J1
Kartenbett

Maßstab: 1:1

L 9537-7008.00 /2

REPLACES: 9537-7008.00 rev.3

Ersatz. Vorausg.:

Endnotes to Wiring Sheets of UTI-1 Motherboard

Note: Unless otherwise stated, all lines connect to the same numbered pins on slots 1 through 15. Ground lines connect between all slots except where noted in endnote 6).

1) The pairs of lines BU1 1A/2A and BU1 1B/2B are designed to handle up to 150 volts from external sources. BU1 pins 2A and 2B are connected together for all the 15 slots.

   If the W&G Analog Module (BN9537/00.03 is installed in the UTI-1, these lines may be used to connect voltages from external power supplies to the motherboard. Jumpers on the Analog Module will have to be installed to connect these voltages through to the motherboard. These jumpers are not installed at the factory. See the description of the Analog Module for details.

   The factory markets a Ringing Generator that interfaces to the UTI-1 through the W&G Analog Module (9537/00.03). When the Ringing Generator and Analog Module with the appropriate jumpers as mentioned in the above paragraph are installed, these lines are dedicated to the voltages produced by the Ringing Generator (Ringing AC, Ringing DC) and the external high voltage power supplies (75 Volts, +150 Volts, -150 Volts) needed to provide the ringing functions.

   An external 15 Volt source can be connected through these lines for use on UTI-1 boards featuring "pin electronics" hybrids.

2) If the W&G Analog Module (9537/00.03) is installed in the UTI-1, these lines may be used to connect voltages from up to eight independent external power supplies from the rear panel to the motherboard. The voltage lines are provided in pairs to provide floating voltages. Jumpers on the Analog Module will have to be installed to connect these voltages through to the motherboard. These jumpers are not installed at the factory. See description of the Analog Module for details.

   Relays on the Analog Module control the connection of these voltages. The voltage pairs designated V1 and V4 have independent relays. The connection of V5 and V6 are controlled together, and the connection of V7 and V8 are controlled together.

   If the power supplies provide sense lines, provisions must be made to connect them to the voltage lines on the Interchangeable Test Adapter (ITA). If these connections are made on the personality board, care must be taken to prevent the output voltages from rising when the ITA is removed (breaking the connection between the voltage and sense lines). This may be accomplished, for example, by installation of low value resistors installed between voltage and sense lines near the power supplies.

3) These lines connect to all slots, 0 through 15, and are hardwired to the internal 175 watt regulated power supply in the UTI-1. See Section 2 of this manual for the specifications of the individual voltages.

4) If the Ringing Generator is connected through the W&G Analog Module (BN9537/00.03), these lines provide certain control functions for the Ringing Generator. One of these, the Interlock (BU1 pin 18A) must be connected to ground to allow the Ringing Generator to output voltages. Jumpers on the Analog Module will have to be installed to connect these lines through the motherboard. These jumpers are not installed at the factory. See the description of the Analog Module for more details.

5) When the W&G Standard Latch Module (9537/00.24) is installed, these pins are used by the two Parametric Test Busses for pin electronic tests. These busses connect voltage and current sources from other UTI-1 pc boards to individual pins of the device

under test on the personality board. One bus can provide the source voltage or current while the other can be used to sense the effect on another test pin.

6) These grounds do not extend to slot 0.

7) UNBALANCED BUS LINES: These lines may be used for any unbalanced digital or analog signal which is less than 35 volts. These lines are shielded on both sides and above and below. They extend from slot 1 through slot 15.

8) These lines connect to the W&G Digital Interface board (if installed). Jumpers must be installed on the Digital Interface if these lines are to be used as Fixture Clock and Strobe. In a PCM application, these lines would be needed to provide clock and strobe to the system if they originate on a board in the UTI-1. A foreseeable application would be the inclusion of a synthesizer board to provide the clock and strobe.

9) The daisy chained lines 0 to 16 connect between adjacent pairs of cards in slots 1 through 15. A connection at an "A" pin will connect to the adjacent slot at a "B" pin. This arrangement allows signals to be used by a limited number of cards, and the same lines can be used for other signals between different cards. For example, a signal generated on a card in slot 3 can be put onto Daisy Chain Bus 5 by connecting to BU1 pin 31A. This signal can be picked up by the card in slot 4 by connecting to BU1 pin 31B. The signal will only be passed to the card in slot 5 if the card in slot 4 connects this signal to BU1 pin 31A.

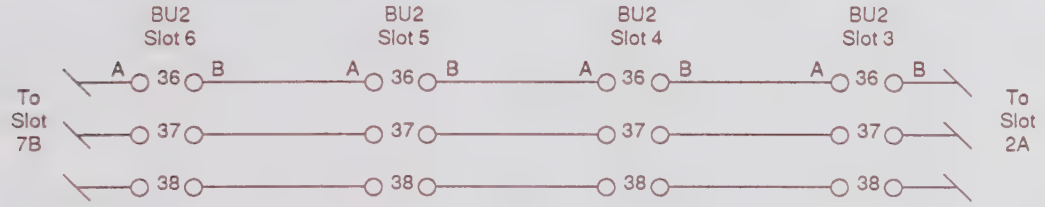


Figure 1 Daisy Chained Bus Wiring Example

In ISDN testing applications, these lines are dedicated for digital transmit signals originating in the Pattern Generators.

10) CLK1- and CLK1+ are adjacent bus lines running between all the slots except slot 0. These clock lines may be used as a differential pair and are primarily intended to synchronize clocks between microprocessors installed on the various UTI-1 boards.

In ISDN testing applications, these lines are dedicated as individual clock lines which are labelled CLK-1 and CLK-2 and originate in the Pattern Generators.

11) CLK2- and CLK2+ are adjacent bus lines running between all the slots including slot 0. These clock lines may be used as a differential pair and are primarily intended to synchronize clocks to the clock on the controller board.

12) The designations show lines which are used when the Parallel Bus Interface Module is installed in slot 0. These include 16 address lines, 16 bidirectional data lines, an address strobe ($\overline{AS}$), an upper data strobe ($\overline{UDS}$), and a lower data strobe ($\overline{LDS}$) and ($\overline{RESET}$). Additionally, there are three handshaking lines that send information from UTI-1 cards to the system controller. These are bus busy ($\overline{BBSY}$), interrupt request ($\overline{IR}$), and data acknowledge ($\overline{DTACK}$). Two trigger lines, ($\overline{TRIGGER\ 1}$) and ($\overline{TRIGGER\ 2}$), and a module interrupt line (INTM) are included for those signals originating on the parallel Bus Interface Module.

The circuitry on each of the other UTI-1 boards must not present more than one standard TTL load. Those lines that pass information to the Parallel Bus Interface Module (the data bus, $\overline{BBSY}$, $\overline{IR}$, and $\overline{DTACK}$) must be able to be tristated on each UTI-1 board using these lines. In addition, driver circuitry on these UTI-1 boards must be able to drive the termination and line impedance (approximately 100 ohms).

Notes in parentheses indicate connections to a resistance package installed on the motherboard containing the line terminations. All the lines except those that pass information only to the controller card are terminated on the motherboard near slot 13. Those lines not terminated on the motherboard will be terminated on the Parallel Bus Interface Module. See Figure 2 for termination details.

Note: $\overline{RESET}$, $\overline{TRIGGER\ 1}$, and $\overline{TRIGGER\ 2}$ are used by both the IEEE Interface Module and the Parallel Bus Interface Module.

13) The Analog Module (9537/00.03) has two 50/75 ohm coaxial connectors on its rear panel that connect to these motherboard lines. Relay contacts are placed on the Analog Board to isolate these lines.

14) These are designed to provide 8 balanced busses for analog signals (up to 620 KHz). Each bus consists of three lines, a ground or shield, a Tip line and a Ring line. The Tip and Ring designations conform to telephone terminology and represent the hot and return lines of a balanced bus. These lines on the motherboard have been specifically designed to minimize cross-talk. They simulate twisted pairs by crossing between layers as they proceed from slot to slot across the motherboard.

15) These designations show lines which are used when the IEEE Interface Module is installed in slot 0. The IEEE Interface Module translates commands from the System Controller to signals that control circuitry on the other UTI-1 boards. The card selects, position lines, and the talk lines are used to write data to a particular card. The card selects, position lines, and listen lines are used to send information from a particular card to the System Controller. These lines are all terminated on the motherboard. Each UTI-1 board that connects to these signals must provide buffering and the ability to tristate the listen lines.

Notes in parentheses indicate connections to a resistance package installed on the motherboard containing the line termination details. All lines except those that pass information only to the controller card are terminated on the motherboard near slot 13. Those lines not terminated on the motherboard will be terminated on the Parallel Bus Interface Module.

Note: $\overline{RESET}$, $\overline{TRIGGER\ 1}$, and $\overline{TRIGGER\ 2}$ may be used by both the IEEE Interface Module and the Parallel Bus Interface Module.

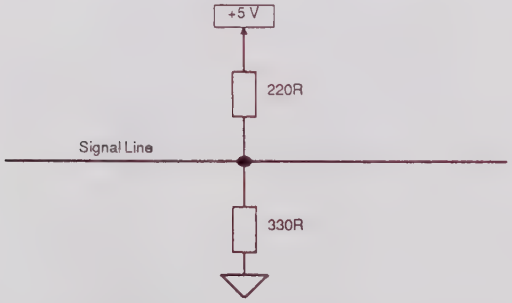


Figure 2 Motherboard Terminations

16) The CARD SELECT LINES allow the controller card in slot 0 to address a particular card in slot 1 through 15. Card Select 1 through Card Select 15 originate at slot 0 (controller card) and connect to BU2 pin 50B of each of the corresponding slots 1 through 15. There is no connection at BU2 pin 50B at slot 0. Circuitry on the controller card in slot 0 allows only one of these lines to go low at a time.

17) In ISDN testing applications, these lines are dedicated to the Record signals for the Pattern Generator/Recorders.

18) In ISDN testing applications, these lines are dedicated to signals necessary for the Pattern Generator/Recorder operation. These signals consist of the Delayed Clock (DEL CK), the Delayed Strobe (DEL STB), External Start (EXT STR), the PCM Shift-in Clock (SHIFT CK), and the Signal Frame ($\overline{SF}$).

WANDEL & GOLTERMANN TECHNOLOGIES, INC.
FIXTURE MAINFRAME

BN 9537 ********** LIST OF REPLACEABLE PARTS ********** SERIES: ALL
DATE: Jan 8, 1990

DIAG REF	ITEM	QTY	PART NUMBER	DESCRIPTION	STOCK LOCATION	VERS/OPT	SERIES STRT	SERIES END	SUBASSEMBLY 9537-XXXX	SUBASSEMBLY CODE
						01			0000	S
	0	0	9537-0000.004	FIX. MAIN FR. COMPL		01			0000	A
	0	1	9537-0100.001	COMPL MAIN FR. ASSY		01			0000	A
	1	1	0700-1310.006	TOP COVER PERF 19"		01			0000	
	2	1	0700-1710.004	COVER BOTTM PERF 19"		01			0000	
	3	2	0700-6000.078	PNL SIDE #6 PAINT		01			0000	
	4	4	0700-0000.016	FOOT SIDE PANEL		01			0000	
	6	2	0700-0000.029	FOOT RIGHT		01			0000	
	7	2	0700-0000.032	FOOT LEFT		01			0000	
	12	4	0000-0421.090	FOOT PLAS BLACK 19"		01			0000	
	13	2	0700-0100.013	GUIDE		01			0000	
	17	1	9537-0000.017	LABEL UTI-1		01			0000	
	18	2	0700-0001.002	HANDLE SIDE PANEL		01			0000	
	20	1	0000-7573.629	CABLE K196 POWCORD G		01			0000	

WANDEL & GOLTERMANN TECHNOLOGIES, INC.
MAINFRAME COMPLETE

SERIES: ALL

BN 9537 ********** LIST OF REPLACEABLE PARTS ********** DATE: Jan 8, 1990

DIAG REF	ITEM	QTY	PART NUMBER	DESCRIPTION	STOCK LOCATION	VERS/OPT	SERIES STRT	SERIES END	SUBASSEMBLY 9537-XXXX	CODE
						01			0100	S
	0	0		COMPL MAINF ASSY	9537-0100.00	01			0100	A
	1	1	9537-7008.009	MOTHER BD ASSY		01			0100	A
	2	1	9537-0200.008	FIX MAIN FR MCH ASSY		01			0100	A
	3	1	9537-0300.005	POWER SUPPLY ASSY		01			0100	A
	7	1	9537-9301.005	RECEIVER ROLL CAM		01			0100	
	8	8	0000-7593.743	SCRW M4X40 ALLEN/RAW		01			0100	
	9	1	9537-0100.166	PANEL FRONT MACHINED		01			0100	
	14	1	9000-0000.159	LABEL SERIAL-MODEL #		01			0100	
	15	16	9537-0200.079	CARD GUIDE TOP		01			0100	

WANDEL & GOLTERMANN TECHNOLOGIES, INC.
FIXTURE MAINFRAME MACH. ASSEMBLY

BN 9537 ********** LIST OF REPLACEABLE PARTS **********

SERIES: ALL
DATE: Jan 8, 1990

DIAG REF	ITEM	QTY	PART NUMBER	DESCRIPTION	STOCK LOCATION	VERS/OPT	SERIES STRT	SERIES END	SUBASSEMBLY 9537-XXXX	SUBASSEMBLY CODE
						01			0200	S
	0	0	9537-0200.008	FIX MAIN FR MCH ASSY		01			0200	A
	1	1	9537-0200.011	PANEL SIDE LEFT		01			0200	
	2	1	9537-0200.024	PANEL SIDE RIGHT		01			0200	
	3	1	9537-0200.037	BAR REAR LOWER		01			0200	M
	4	1	9537-0200.040	BAR FRONT LOWER		01			0200	
	5	1	9537-0200.053	BAR REAR TOP		01			0200	
	6	1	9537-0200.066	BAR FRONT TOP		01			0200	
	8	16	9537-0200.110	ROD CAM		01			0200	M
	16	1	9537-0200.095	STRIP TRIM LEFT		01			0200	
	17	1	9537-0200.147	STRIP TRIM RIGHT		01			0200	
	18	1	0700-0000.333	BOX FOR ACCESSORIES		01			0200	
	19	16	9537-0200.121	FLAG CAM		01			0200	
	20	16	9537-0200.134	DRIVER CAM		01			0200	
	31	1	0001-0020.782	FUSE 2A FAST 5X20mm		01		C	0200	
	31	2	0000-7657.809	FUSE 5A FAST 5X20mm		01	D		0200	
	38	1	9537-0200.192	PANEL REAR LOW.,MRKD		01			0200	M

WANDEL & GOLTERMANN TECHNOLOGIES, INC.

POWER SUPPLY ASSEMBLY

SERIES: ALL

BN 9537 ********** LIST OF REPLACEABLE PARTS ********** DATE: Jan 8, 1990

DIAG REF	ITEM	QTY	PART NUMBER	DESCRIPTION	STOCK LOCATION	VERS/OPT	SERIES STRT	SERIES END	SUBASSEMBLY 9537-XXXX	SUBASSEMBLY CODE
						01			0300	S
		5	0001-0030.675	SLEEVE SOLDER SZ 2		01			0300	
	0	0		POWER SUPPLY ASSY	9537-0300.00	01			0300	A
	1	1		POWER SUPPLY +-15V 5	XX12-0013.00	01		C	0300	
	1	1		PWR SPLY 5/15/-15V	XX12-0024.00	01	D	D	0300	
	1	1		PWR SUPPLY +5V +-15V	XX12-0026.00	01	E		0300	
	7	1	9537-0300.021	HOUSING POWER SUPPLY		01			0300	
	8	1	9537-0300.157	PLATE INSULATOR		01	D		0300	
	10	7		CAP F-THRU 4700pF500	XX02-0015.00	01	D	D	0300	
	10	9		CAP F-THRU 4700pF500	XX02-0015.00	01	E		0300	
	11	7	0855-0038.016	RING NUT M7 F5		01	D	D	0300	
	11	9	0855-0038.016	RING NUT M7 F5		01	E		0300	
	14	2		RECEPT CRIMP AU F1P	XX03-0070.00	01			0300	
	15	1		HOUSING RECEPT F1X4P	XX03-0386.00	01			0300	
	19	1	0001-0068.867	COVER FUSE BLK PJM 1		01			0300	
	21	1	9537-0300.063	PANEL REAR MARKED PS		01		C	0300	
	21	1	9537-0300.131	PANEL REAR MARKED PS		01	D		0300	M
	22	1		LUG SOLDER BENT #6	XX27-0008.00	01			0300	
	27	1	0001-0020.805	FUSE 2.0A SLO 5X20mm		01		C	0300	
	29	1	0001-0034.723	HOLDER FUSE W/O CAP		01			0300	
	30	1	0615-8003.005	SWITCH ON/OFF POWER		01			0300	
	31	1	0427-0041.002	HOUSING SWITCH		01			0300	
	37	1	0427-0040.016	COVER SW/HOUS		01			0300	
	38	1	0000-7554.656	CAP SWITCH FA 101		01			0300	
	42	1	9537-0300.050	COVER POWER SUPPLY		01	C		0300	
	45	2	9537-0300.102	SHIELD INSULATOR		01	D		0300	
	46	1	9537-0300.092	BRACKET LINE FILTER		01	D		0300	
	48	6		STANDOFF PEM M3X7.5	XX24-0073.00	01	D		0300	
	58	1	9537-0300.047	BRACKET FAN MOUNTING		01		C	0300	
	60	1	9537-0300.128	COVER PWR SUPPLY MRK		01	D	D	0300	M
	60	1	9537-0300.173	COVER PWR SUPPLY MRK		01	E		0300	M
	74	1		LABEL CAUTION HIVO L	XX21-0043.00	01			0300	
F	1	1	0001-0020.782	FUSE 2A FAST 5X20mm		01		C	0300	
F	1	1	0000-7657.809	FUSE 5A FAST 5X20mm		01	D		0300	
FI	1	1		FILTER PWR PNL MT	XX15-0129.00	01			0300	

WANDEL & GOLTERMANN TECHNOLOGIES, INC.
MOTHER BOARD ASSEMBLY

BN 9537 ********** LIST OF REPLACEABLE PARTS ********** SERIES: ALL
DATE: Jan 8, 1990

DIAG	REF	ITEM	QTY	PART NUMBER	DESCRIPTION	STOCK LOCATION	VERS/OPT	SERIES STRT	SERIES END	SUBASSEMBLY 9537-XXXX	SUBASSEMBLY CODE
							01			7000	S
		0	0		MOTHER BOARD ASSY	9537-7000.00	01			7000	A
		1	1	9537-7000.025	PC BOARD MACHINED		01			7000	
		2	32		CONN EDGE ZIF 2X50P	XX03-0507.00	01			7000	
		8	8	0000-2901.026	TERM SOLD WN34/5/8		01		D	7000	
		8	10	0000-2901.026	TERM SOLD WN34/5/8		01	E		7000	
		9	4	0000-7570.999	HEADER STR PC M1X4P		01			7000	
		10	4		INSUL THERM TIP-32 C	XX28-0151.00	01			7000	
		13	4		BUSHING NYL TO220 MT	XX28-0154.00	01			7000	
		52	1	0001-0072.468	LABEL YEL/BLK C-MOS		01			7000	
00	C	1	1		C TANT 100uF 10%20V	XX32-0090.00	01		C	7000	
00	C	1	1		C-ELYT TA 330UF 30V	XX32-0129.00	01	D		7000	
00	C	2	1		C TANT 100uF 10%20V	XX32-0090.00	01		C	7000	
00	C	2	1		C-ELYT TA 330UF 30V	XX32-0129.00	01	D		7000	
00	C	3	1		C TANT 100uF 10%20V	XX32-0090.00	01		C	7000	
00	C	3	1		C-ELYT TA 330UF 30V	XX32-0129.00	01	D		7000	
00	C	4	1	0000-7594.425	C-CER 220N 10% X 50V		01	D		7000	
00	C	5	1	0000-7594.425	C-CER 220N 10% X 50V		01			7000	
00	C	6	1	0000-7594.425	C-CER 220N 10% X 50V		01			7000	
00	C	7	1		C-ELYT TA 330UF 30V	XX32-0129.00	01			7000	
00	C	8	1		C-ELYT TA 330UF 30V	XX32-0129.00	01			7000	
00	C	9	1		C-ELYT TA 330UF 30V	XX32-0129.00	01			7000	
00	C	10	1		C-ELYT TA 330UF 30V	XX32-0129.00	01			7000	
00	C	11	1		C TANT 100uF 10%20V	XX32-0090.00	01		C	7000	
00	C	11	1		C-ELYT TA 330UF 30V	XX32-0129.00	01	D		7000	
00	C	12	1		C TANT 100uF 10%20V	XX32-0090.00	01		C	7000	
00	C	12	1		C-ELYT TA 330UF 30V	XX32-0129.00	01	D		7000	
00	C	13	1		C TANT 100uF 10%20V	XX32-0090.00	01		C	7000	
00	C	13	1		C-ELYT TA 330UF 30V	XX32-0129.00	01	D		7000	
00	C	14	1		C TANT 100uF 10%20V	XX32-0090.00	01		C	7000	
00	C	14	1		C-ELYT TA 330UF 30V	XX32-0129.00	01	D		7000	
00	C	15	1		C TANT 100uF 10%20V	XX32-0090.00	01		C	7000	
00	C	15	1		C-ELYT TA 330UF 30V	XX32-0129.00	01	D		7000	
00	C	16	1		C TANT 100uF 10%20V	XX32-0090.00	01		C	7000	
00	C	16	1		C-ELYT TA 330UF 30V	XX32-0129.00	01	D		7000	
00	C	17	1	0000-7594.425	C-CER 220N 10% X 50V		01			7000	

WANDEL & GOLTERMANN TECHNOLOGIES, INC.
MOTHER BOARD ASSEMBLY

BN 9537 ********** LIST OF REPLACEABLE PARTS ********** SERIES: ALL DATE: Jan 8, 1990

DIAG	REF	ITEM	QTY	PART NUMBER	DESCRIPTION	STOCK LOCATION	VERS/OPT	SERIES STRT	SERIES END	SUBASSEMBLY 9537-XXXX CODE
							01			7008
08	C	18	1	0000-7594.425	C-CER 220N 10% X 50V		01			7008
08	C	19	1	0000-7594.425	C-CER 220N 10% X 50V		01			7008
08	C	20	1	0000-7594.425	C-CER 220N 10% X 50V		01			7008
08	C	21	1	0000-7594.425	C-CER 220N 10% X 50V		01			7008
08	C	22	1	0000-7594.425	C-CER 220N 10% X 50V		01			7008
08	GL	1	1		ZENER 1N5347B 10V+5%	XX37-0182.00	01			7008
08	GL	2	1		ZENER 1N5347B 10V+5%	XX37-0182.00	01			7008
08	GL	3	1		ZENER 1N5347B 10V+5%	XX37-0182.00	01			7008
08	GL	4	1		ZENER 1N5347B 10V+5%	XX37-0182.00	01			7008
08	IC	1	1	0000-7569.955	IC VREG LM317 T220		01			7008
08	IC	2	1	0000-7569.955	IC VREG LM317 T220		01			7008
08	IC	3	1	0000-7569.955	IC VREG LM317 T220		01			7008
08	IC	4	1	0000-7569.955	IC VREG LM317 T220		01			7008
08	L	1	1	0001-0042.689	COIL 5uH B82501-B-C2		01			7008
08	L	2	1	0001-0042.540	COIL 10uH 20% 3A		01		C	7008
08	L	2	1		COIL PWR 47U 15%	XX33-0158.00	01	D		7008
08	L	3	1	0001-0042.540	COIL 10uH 20% 3A		01		C	7008
08	L	3	1		COIL PWR 47U 15%	XX33-0158.00	01	D		7008
08	L	4	1	0001-0042.689	COIL 5uH B82501-B-C2		01	E		7008
08	R	1	1	0000-7643.415	R-MF 14.3R 1% 204		01		C	7008
08	R	1	1	0000-7643.224	R-MF 8.66R 1% 204		01	D		7008
08	R	2	1	0000-7643.415	R-MF 14.3R 1% 204		01		C	7008
08	R	2	1	0000-7643.224	R-MF 8.66R 1% 204		01	D		7008
08	R	3	1	0000-7643.415	R-MF 14.3R 1% 204		01		C	7008
08	R	3	1	0000-7643.224	R-MF 8.66R 1% 204		01	D		7008
08	R	4	1	0000-7643.415	R-MF 14.3R 1% 204		01		C	7008
08	R	4	1	0000-7643.224	R-MF 8.66R 1% 204		01	D		7008
08	R	5	1	0000-7608.890	R-MF 221 OHM 1% 204		01	D		7008
08	R	6	1	0000-7519.484	R-MF 332 OHM 1% 204		01	D		7008
08	RN	2	1		R-PACK 6X221/331 OHM	XX08-0696.00	01			7008
08	RN	4	1		R-PACK 6X221/331 OHM	XX08-0696.00	01			7008
08	RN	6	1		R-PACK 6X221/331 OHM	XX08-0696.00	01			7008
08	RN	8	1		R-PACK 6X221/331 OHM	XX08-0696.00	01			7008
08	RN	10	1		R-PACK 6X221/331 OHM	XX08-0696.00	01	D		7008
08	RN	12	1		R-PACK 6X221/331 OHM	XX08-0696.00	01	D		7008
08	RN	14	1		R-PACK 6X221/331 OHM	XX08 0696.00	01	D		7008

WANDEL & GOLTERMANN TECHNOLOGIES, INC.

MOTHER BOARD ASSEMBLY

BN 9537 ********** LIST OF REPLACEABLE PARTS ********** SERIES: ALL

DATE: Jan 8, 1990

DIAG	REF	ITEM	QTY	PART NUMBER	DESCRIPTION	STOCK LOCATION	VERS/OPT	SERIES STRT	SERIES END	SUBASSEMBLY 9537-XXXX	SUBASSEMBLY CODE
08	RN	16	1		R-PACK 6X221/331 OHM	XX08-0696.00	01	D		7008	

4. UTI-1 Module Design Guidelines

Contents **Page**

4.1. Physical Guidelines 4.1-1

4.2. Standard Mechanical Parts 4.2-1

4.3. Electrical Guidelines 4.3-1

4.3.1 +5V, +15V, and -15V Power Limitations 4.3-1

4.3.2 Signal Loading and Drive Requirements 4.3-5

4.3.3 Selecting Between the 4 bit and 16 Bit Parallel Bus 4.3-7

4.3.4 Simple Four Bit Parallel Bus Interfacing Circuitry Details 4.3-7

4.3.4.1 $\overline{\text{Card Select}}$, $\overline{\text{Talk}}$/Listen and Position Line POS 2^3 . . . . . .4.3-7

4.3.4.2 Relationship Between Input Lines of the Parallel Latches . . .4.3-7

4.3.5 Complex Four Bit Parallel Bus Interfacing Circuitry Details 4.3-8

4.3.5.1 $\overline{\text{Card Select}}$, $\overline{\text{Talk}}$/Listen and Position Line POS 2^3 . . . . . .4.3-8

4.3.5.2 Relationship Between Input Lines of the Parallel Latches (Talk Circuitry) 4.3-13

4.3.5.3 Listen Circuitry 4.3-13

4.3.5.4 Examples of Using the Talk Circuitry 4.3-13

4.3.5.5 Examples of Reading Data Back to the Controller 4.3-14

4.3.6 Sample Sixteen Bit Parallel Bus Interfacing Circuitry 4.3-14

4.3.7 Cable Shielding 4.3-16

4.3.8 Module Identification Number 4.3-16

4. Module Design Guidelines

With the aid of this section, an experienced hardware designer can create custom interface modules for use in the UTI-1. For proper operation of such modules, great care must be taken to conform to both the physical and electrical specifications.

4.1. Physical Guidelines

The physical dimensions of any module designed for the UTI-1 are extremely important. The module must be correctly fitted to insure proper electrical connections on the UTI-1 motherboard and the front connector of the Interchangeable Test Adapter.

The UTI-1 can fit up to 15 single width modules; however, some modules may need to be designed for double width. This gives additional space for mounting more or larger connectors on the rear panel. See Figure 4.1.b for the dimensions of the single and double width rear panels.

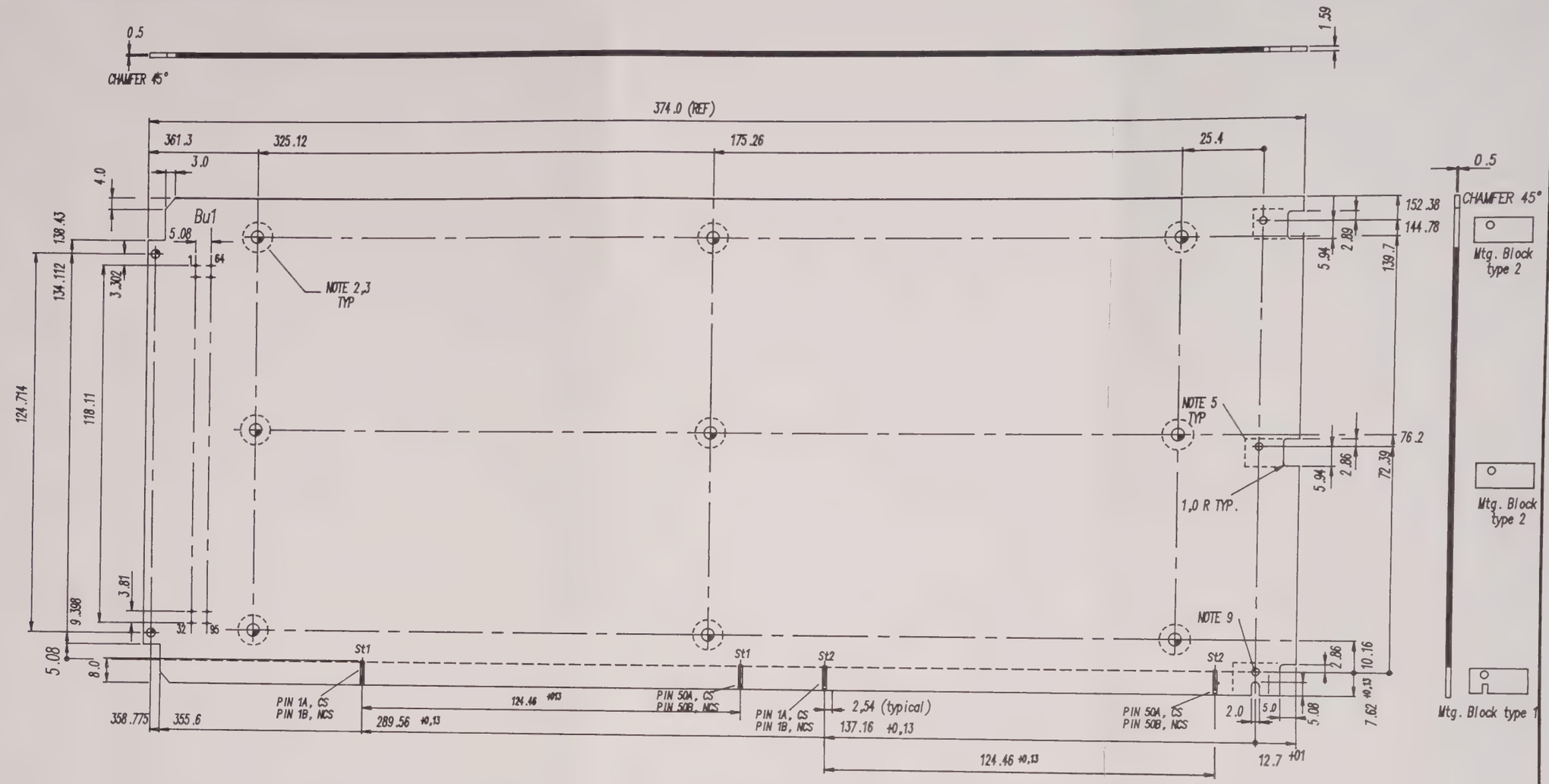
See figure 4.1.a for the recommended dimensions. Section 4.2. of this manual contains some of the standard mechanical parts which can be used.

Notes: For Figure 4.1.a

1) All tolerances are 0.25mm unless otherwise specified.
2) Mount no components and run no tracks (copper) in the following areas:
   a) 4.0mm from card top, used by card guides.
   b) 8.0mm from bottom, excluding connector finger.
   c) 10.0 mm diameter area around 4.2 mm diameter holes (see note 3).
   d) 27mm from front end of board (ITA connection) toward rear on straight line across entire width of board. Lands are allowed in this area.
3) 4.2 holes shown are optional. They are to be provided only when cover shield is mounted on P.C. board. Connect all 4.2 holes to ground and provide 1.6mm of copper around the hole on CS and NCS. (Pad size 7.4 mm diameter, 0.3 inches diameter)
4) Tolerances are non-accumulative on linear dimensions.
5) P.C board must be grounded to each rear panel mounting block.
6) Maximum component height is 17.5mm for single width modules and 36mm for double width boards on component side and 3.5mm on non-component side.
7) Solder mask both sides using DEXTER HYSOL 1000, PC-401 or equivalent.
8) Connector fingers of St1 and St2 are on .1 grid with a copper pad width of 1.59mm (.062"). Use Bishop Graphics Inc. type 6811 connector strips for art work. (St1 & St2).
9) Use this hole as datum hole.
10) This dimension must also be shown on the "MACHINED" drawing. Also show two connector fingers and related information.
11) Unless otherwise specified, keep all copper at least 1.27mm away from all outside routing edges. (See note 2).
12) Provide no solder mask under rear panel mounting blocks.

Terminology

CS	Component side of PC board.
NCS	Non-component side of PC board.



NOTES:

1) All tolerances are 0,25mm unless otherwise specified.

2) Mount no components and run no tracks (copper) in following areas: a) 4,0mm from card top, used by card guids. b) 8,0mm from bottom; excluding connector fingers. c) 10,0 0 area around 4,2 0 holes (see note 3). d) 27mm from front end of board toward rear on straight line across whole width of board; lands are o.k. in this area

3) 4,2 Holes shown are optional. To be provided only when cover shield to be mounted on P.C. Board. Connect all 4,2 holes to ground & provide 1,6mm of copper around the hole on CS & NCS. (7.4mm dia. ±.3" dia.)

4) Tolerances are non-accumulative on linear dimensions.

5) P.C. Board must be grounded to each rear panel mounting block.

6) Maximum component height is 17,5mm on component side and 3,5mm non-component side.

7) Soldermask both sides using DEXTER HYSOL 1000, PC-401 OR EQUIVALENT. OVER BARE COPPER.

8) Fingers of St1 and St2 are on .1 grid with a copper pad width of 1,59mm (.062"). Use Bishop graphics Inc. type 6811 connector strips for artwork. (St1 & St2).

9) Use this hole as datum hole

10) This dimension must also be shown on the "MACHINED" drawing. Also show two fingers & related info.

11) Unless otherwise specified, keep all copper at least 1.27mm away from all outside routing edges. (see note 2).

12) Provide no solder mask under rear panel mounting blocks.

HOLES

0 4.2 (AFTER PLATING) see note 3

0 3.0 (AFTER PLATING) this hole not on grid.

0 2.5 (AFTER PLATING)

0 0.9 (AFTER PLATING) this hole is on grid

AREA TO BE GOLD PLATED (50u in Hard gold over 100u in Nickel or equivalent.)

FIG: 4.1.0

Oberflächen/Finish:

Anz. Issue	Änderung Change	Tag Date	Name
1	NEW	3-21	MRM

Darstellung Methode E — First Angle Projection

	Tag Date	Name
88'		
Bearb. Drawn	3-21	MANRIQUEZ
Gepr. Check		

WANDEL & GOLTERMANN, INC. Electronic Measurement Technology, Research Triangle Park, North Carolina

Halbzeug und Werkstoffe/Material: Base laminate FR4 Thin clad laminate 1 oz copper all sides B Stage FR4-116 or equivalent 1.59 (.062") THK

Benennung/Designation: UTI-1 MODULE OUTLINE

9537-XXXX

Ersatz für/Replaces:

Winkelmasse/Ang. Tol.:

Allgemeintoleranzen/Std. Tol.

Required	Nennmaßbereich/Millimeters 1 bis 6	über 6 bis 30	über 30 bis 180	über 180 bis 300	über 300 bis 1000
	±0.05	±0.1	±0.15	±0.2	±0.3
	±0.1	±0.2	±0.3	±0.5	±0.8
	±	±	±	±	±

Vertreter Distribution: USA — Massstab Scale: N/A — Page 1 of 1

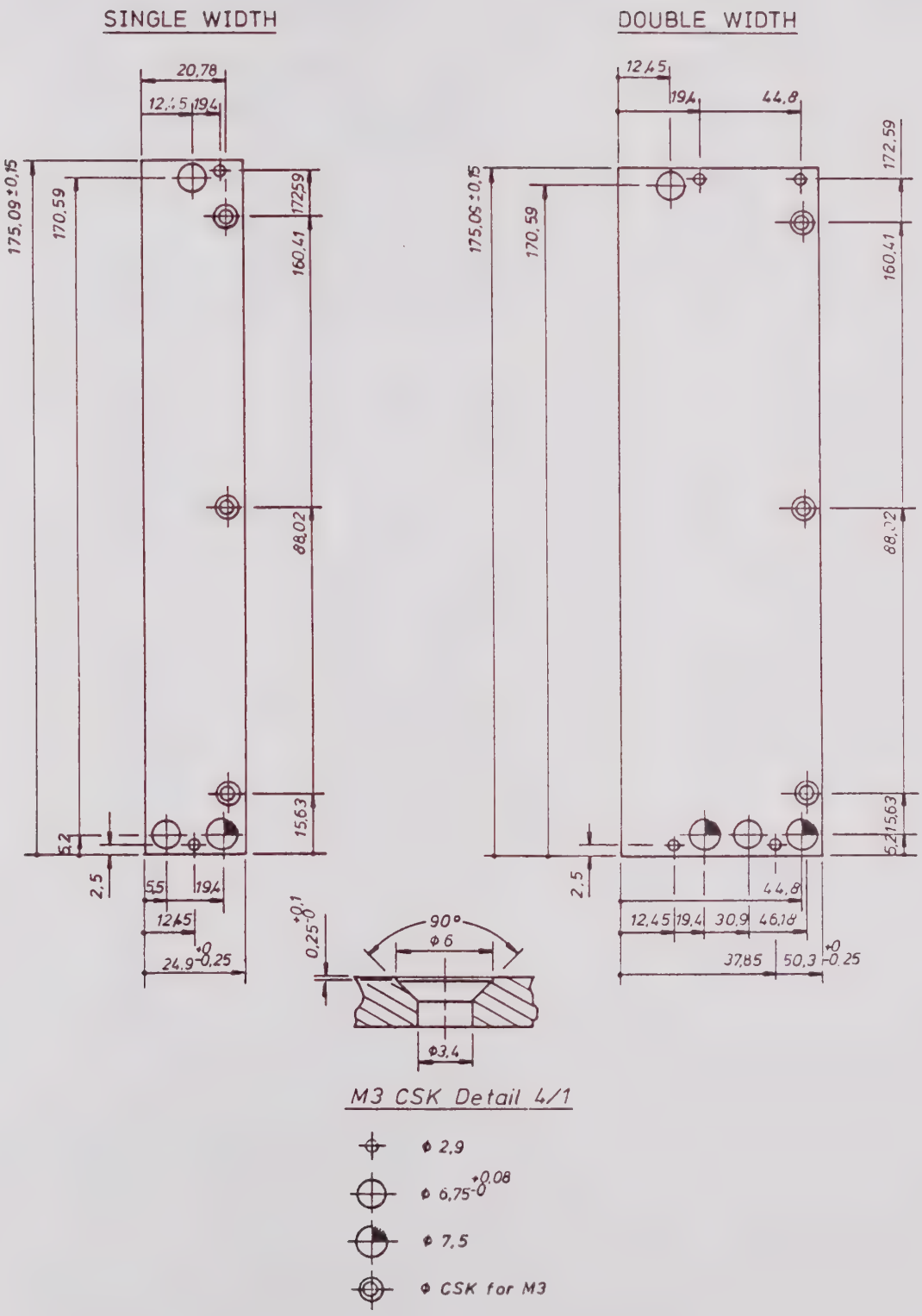


Figure 4.1.0b Rear Panel Dimensions

4.2. Standard Mechanical Parts

Part Number	Description	Notes
9537-7001.06	Block, Panel Mounting #1	
9537-7001.08	Block, Panel Mounting #2	
XX05-0184.00	Screw, cylinder, slot M2.5x6	For mounting block on board
XX05-0215.00	Screw, countersink, cross slot M3x6	For mounting block on panel
XX03-0512.00	Connector W/O pins,64 pin	
XX03-0518.00	Receptacle pin angle, row 3	
XX03-0517.00	Receptacle pin angle, row 1	

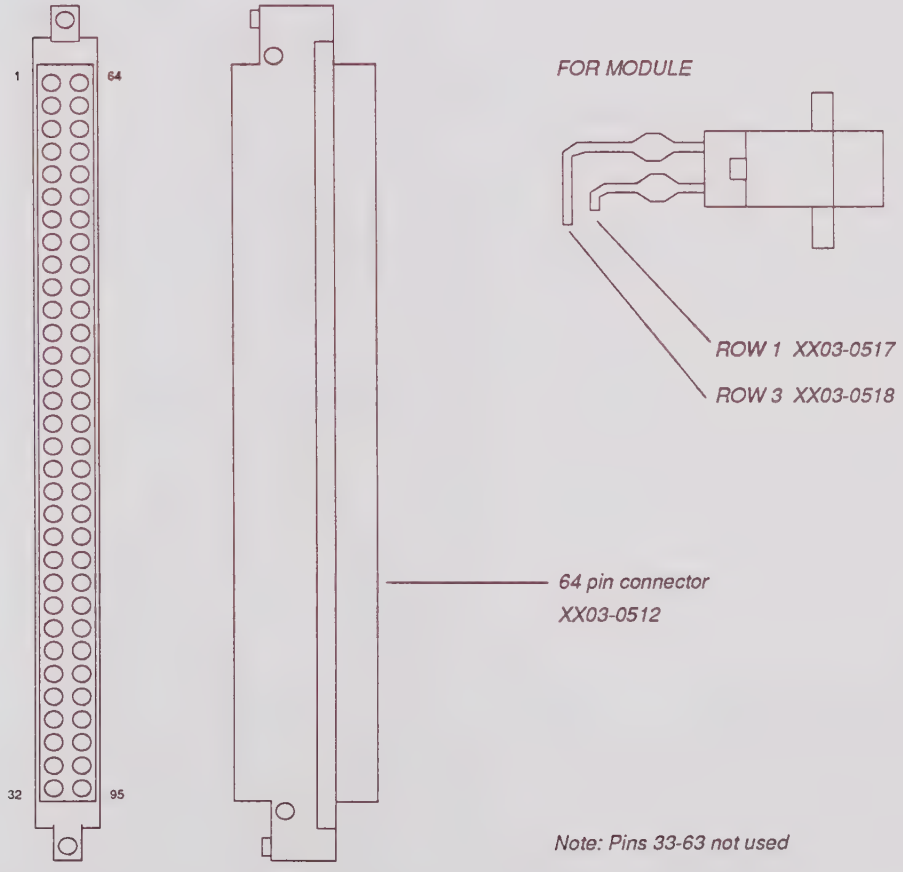


Figure 4.2. 64 pin connector details

4.3. Electrical Guidelines

4.3.1 +5V, +15V, and -15V Power Limitations

When designing UTI-1 modules, the combined output power must not exceed its maximum allowed value, and the +5V, -15V, and +15V individual power ratings must not be exceeded.

Refer to the Standard Module Power Consumption table in this section to insure that power consumption limits are not exceeded.

The motherboard provides two +5 volt connections as well as +15 and -15 volt connections to each of the module positions. See the motherboard diagram in section 3 for their location.

Motherboard Power for Modules (Series A - C)

Voltage	Current (Amps)	Power (Watts)
+5	1 to 11	55
+15	0 to 1	15
-15	0 to 1	15

* Total Power not to exceed 75 Watts

Motherboard Power for Modules (Series D...)

Voltage	Current (Amps)	Power (Watts)
+5	0 to 15	75
+15	0 to 4	60
-15	0 to 4	60

* Total Power not to exceed 175 Watts

Standard Module Power Consumption in Watts

Standard Module	+5 Volts	+15 Volts	-15Volts	Total	Notes
9537/00.01 IEEE-488 Int.	8.75		-----	8.75	
9537/00.02 Digital Int.	9.50	-----	-----	9.50	
9537/00.03 Analog Module	6.50 3.00 17.50	0.20 0.20 0.20	0.20 0.20 0.20	6.50 5.90 17.90	1 2 3
9537/00.04 6 × 8 Switch Matrix	6.00 3.75 25.00	----- ----- -----	----- ----- -----	6.00 3.75 25.00	1 2 3
9537/00.06 Custom Termination Module	8.00 5.00 25.00	----- ----- -----	----- ----- -----	8.00 5.00 25.00	1 2 3
9537/00.23 2 × 32 Switch Matrix	5.00 2.50 38.75	----- ----- -----	----- ----- -----	5.00 2.50 38.75	1 2 3
9537/00.24 Standard Latch Module	12.50 4.50 23.75	0.75 0.75 0.75	1.50 1.50 1.50	14.75 6.75 26.00	1 2 3
9537/00.25 Oscilloscope Probe Access Module	2.50 1.50 19.00	2.00 2.00 2.00	0.50 0.50 0.50	5.00 4.00 21.50	1 2 3
9537/00.27 Parallel Bus Ex	8.00	-----	-----	8.00	

Be sure to take into account the power consumption of all modules and the Personality Based Interchangeable Test Adapter.

Notes:

1. Power consumption during normal usage. This power rating should be used in most cases.
2. Power consumption during minimal usage. This power rating should be used when more than one module is used and this is the secondary module or if this module is not fully utilized.
3. Maximum possible power consumption. This condition is not typical, but includes all relays energized and all components utilized under normal loads.

The conditions for the applicable modules under the above conditions are described in the following table.

Analog Module BN 9537/00.03

1. DMM (Bu5), Tx (Bu6), Rx (Bu7), Spare (Bu8), Spare (Bu9), and Spare (Bu10) are connected to the motherboard or Interchangeable Test Adapter. The Tx and Rx ports are set to the single ended mode. V1 through V4 and all Auxiliary Supply voltages are connected to the motherboard or Interchangeable Test Adapter. The AC and DC Auxiliary Supply Voltages are combined.
2. DMM (Bu5), Tx (Bu6), and Rx (Bu7) are connected to the motherboard or Interchangeable Test Adapter. The Tx and Rx ports are set to the balanced mode. V1 through V4 and all Auxiliary Supply voltages are connected to the motherboard or Interchangeable Test Adapter. The AC and DC Auxiliary Supply Voltages are combined.
3. All relays are energized.

6 × 8 Switching Matrix BN 9537/00.04

1. The six motherboard busses (AB1 through AB6) are connected to six of the Interchangeable Test Adapter output channels. The two remaining output channels are terminated.
2. All eight Interchangeable Test Adapter output channels are terminated.
3. All relays are energized.

Custom Termination Module BN 9537/00.06

1. Up to twenty relays are energized. This allows for different combinations of Programmable Decadic Impedances and Complex Impedances.
2. Up to twelve relays are energized. This will allow the connection of two complex impedances in series or parallel with a Programmable Decadic Impedance of no more then 6 relays.
3. All relays are energized.

2 × 32 Switch Matrix Module BN 9537/00.23

1. Two of the input channels from either the motherboard or rear panel are connected to two different Interchangeable Test Adapter output channels. Two additional output channels are terminated.
2. Two of the input channels from either the motherboard or rear panel are connected to two different Interchangeable Test Adapter output channels.
3. All relays are energized.

Standard Latch Module BN 9537/00.24

1. All of the latched talk lines and listen lines are connected to the Interchangeable Test Adapter.
2. Only the permanently connected 32 talk lines are connected to the Interchangeable Test Adapter.
3. All relays are energized.

Oscilloscope Probe Access Module BN 9537/00.25

1. One input channel is connected to Output A, and another input channel is connected to Output B. Both output channels are set to ÷100.
2. One input channel is connected to Output A, and another input channel is connected to Output B. Both output channels are left at the preset mode of ÷10.
3. All relays are energized.

4.3.2 Signal Loading and Drive Requirements

The following signal loading and drive guidelines must be met to ensure reliable data transfers on the parallel bus:

* Do not terminate any signal line. All lines are terminated in the UTI-1 motherboard.
* Printed circuit card trace length for each signal should be kept shorter than three inches. Traces should be narrow and placed as far as possible from power and ground planes.

4 Bit Parallel Bus Receiver and Driver Requirements

Signal Name	Min. Recvr. Loading	Suggested Receiver	Suggested Driver	Note
TALK	1 74LS load	74LS240, 74LS241, 74LS244		
LISTEN			74ALS245A-1, 74ALS244A-1, 74ALS645A-1	1
POSITION	1 74LS load	74LS240, 74LS241, 74LS244		
CARD SELECT $\overline{CS}_1$ - $\overline{CS}_{15}$	1 74LS load	74LS240, 74LS241, 74LS244		2
$\overline{RESET}$	1 74LS load	74LS240, 74LS241, 74LS244		2
$\overline{T}$/L	1 74LS load	74LS240, 74LS241, 74LS244		
$\overline{REM}$/LOCAL	1 74LS load	74LS240, 74LS241, 74LS244		3
ADDR	1 74LS load	74LS240, 74LS241, 74LS244		3

Notes:

1. LISTEN lines must be enabled by the selected module during INTERROGATE control blocks only. These lines must be tristated otherwise.
2. These lines are unique to the UTI-1 motherboard.
3. These lines are unique to the Control Expansion Connector.

16 Bit Parallel Bus Receiver and Driver Requirements

Signal Name	Max. Recvr. Loading	Suggested Receiver	Suggested Driver	Note
A_1 - A_{15}, $\overline{UDS}$, $\overline{LDS}$, INTM, R/$\overline{W}$, $\overline{ADS}$	1 74LS load	74LS244, 74LS245, 74LS240, 74LS241		
$\overline{IR}$, TRIG1, TRIG2, & $\overline{BBSY}$	1 74LS load	74LS244, 74LS240, 74LS241,	7417, 7407, 74S38	1
D_0 - D_{15}	1 74LS load	74LS244, 74LS240, 74LS241,	74ALS245A-1, 74ALS244A-1, 74ALS645A-1 74ALS245A-1, 74ALS244A-1, 74ALS645A-1	2
$\overline{DTACK}$			74ALS245A-1, 74ALS244A-1, 74ALS645A-1	3
$\overline{CS_1}$ - $\overline{CS_{15}}$ $\overline{RESET}$	1 74LS load			

Notes:

1. Open Collector drivers must be used. A pull-up resistor has been provided for these lines on the UTI-1 motherboard and is not necessary on the UTI-1 modules.
2. The data bus should only be driven by the selected slave board during READ cycles and should be tristated at other times.
3. The $\overline{DTACK}$ line should only be driven by the selected slave board and should be tistated by other boards.

Bus Driver Terminology

Totem Pole - is an active driver in both states which sinks current when low and sources current when high. These drivers are used on signals having only a single driver per line.

Tri-state - is an active driver which goes to high impedance when off, sinks current when low, and sources current when high. These drivers are used on lines which can be driven by several devices. Only one of these drivers can be active at any one time.

Open collector - sinks current when low but sources little or no current when high. Pull-up or terminating resistors should be used to ensure that the signal line rises to a high level whenever it is not driven low. These drivers are useful for lines which can be driven by several devices simultaneously.

4.3.3 Selecting Between the 4 bit and 16 bit Parallel Busses

Before designing a UTI-1 module, a decision has to be made to select either the 4 or 16 Bit Parallel Bus for controlling the UTI-1 module. Of the two available computer interfaces, the IEEE Interface module supports only the Four Bit Parallel Bus. The Parallel Bus Interface module supports both the Four Bit Parallel Bus and the 16 Bit Parallel Bus. In general, the interface circuitry for the 4 Bit Parallel Bus is simpler, but the 16 Bit Parallel Bus provides higher speed and much larger addressing capability.

Use the 16 Bit Parallel Bus when high data speeds are required and for real time applications which require smaller, predictable response times. This bus is more suitable for interfacing with UTI-1 modules with on-board microprocessors and peripheral devices. See section 3.4. for more information.

Use the 4 Bit Parallel Bus for modules that require small amounts of data transfer at lower speeds and where response time is not critical. See section 3.2. for in depth information and sample interfacing circuitry for this bus.

4.3.4 Simple Four Bit Parallel Bus Interfacing Circuitry Details

Note: The following discussion refers to figure 4.3.4.

Figure 4.3.4 shows the typical circuitry on a UTI-1 module needed to interface with the 4 Bit Parallel Bus. This circuitry writes to program positions A through H and contains no listen circuitry.

4.3.4.1 $\overline{\text{Card Select}}$, $\overline{\text{Talk}}$/Listen, and Position Line POS 2^3

The $\overline{CS}$ (card select) input line must be low (0 volts) in order for any Four Bit Parallel Bus communication to occur between the system controller and the module. This line pulses low for each program data position. If the POS 2^3 input line is high, the card select signal will be blocked at IC 1.2. POS 2^3 is only used when writing to program position I through P. When POS 2^3 input line is low, the card select pulses will pass through IC 1.2.

When the bus is in the talk mode, the $\overline{T}$/L input line will be low (0 volts). The $\overline{CS}$ (Card Select) pulse will be passed by IC 1.3 to the enable pins of the addressable latch ICs (IC 3, 4, 5, and 6). The talk data will be decoded by these ICs. If the bus is in the listen mode, the $\overline{T}$/L input line will be high and block the card select pulses at IC 1.3.

4.3.4.2 Relationship Between Input Lines of the Parallel Latches

The information latched to the outputs of the addressable parallel latch ICs depends on the information present at the position lines and the talk data lines when a card select pulse reaches the enable pins. The position lines are connected in parallel to all of the addressable latch ICs, and each of the Talk data lines is connected to a different addressable latch IC. IC 3 latches the 2^0 talk data to the appropriate output pins; IC 4 latches the 2^1 talk data to the appropriate output pins; IC 5 latches the 2^2 talk data to the appropriate output pins; and IC 6 latches the 2^3 talk data to the appropriate output pins. The following chart shows the correlation between the code on the position lines and the output pin that the data is latched to.

Pos 2^0	Pos 2^1	Pos 2^2	Pos 2^3	Address
0	0	0	0	A
1	0	0	0	B
0	1	0	0	C
1	1	0	0	D
0	0	1	0	E
1	0	1	0	F
0	1	1	0	G
1	1	1	0	H

4.3.5 Complex Four Bit Parallel Bus Interfacing Circuitry Details

Note: Please refer to Figure 4.3.5 in the following discussion.

Figure 4.3.5 shows typical circuitry used on a UTI-1 module needed to interface with the 4 Bit Parallel Bus. Examples of controllable elements, circuitry to send an eight bit board identification to the system controller, and sample circuitry for sending other data back to the system controller are included. This circuitry uses all program positions A through P.

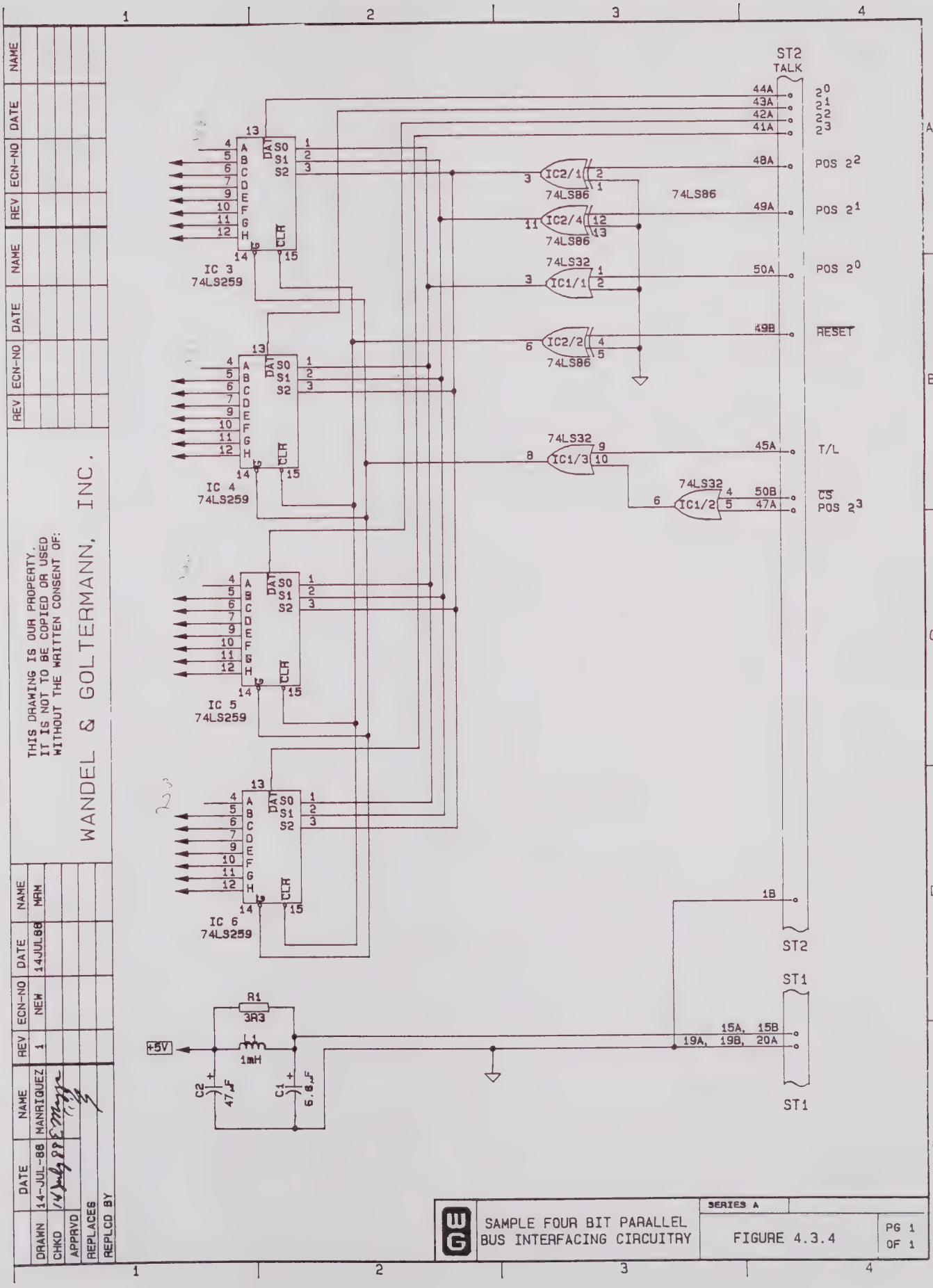
4.3.5.1 $\overline{\text{Card Select}}$, $\overline{\text{Talk}}$/Listen, and Position Line POS 2^3

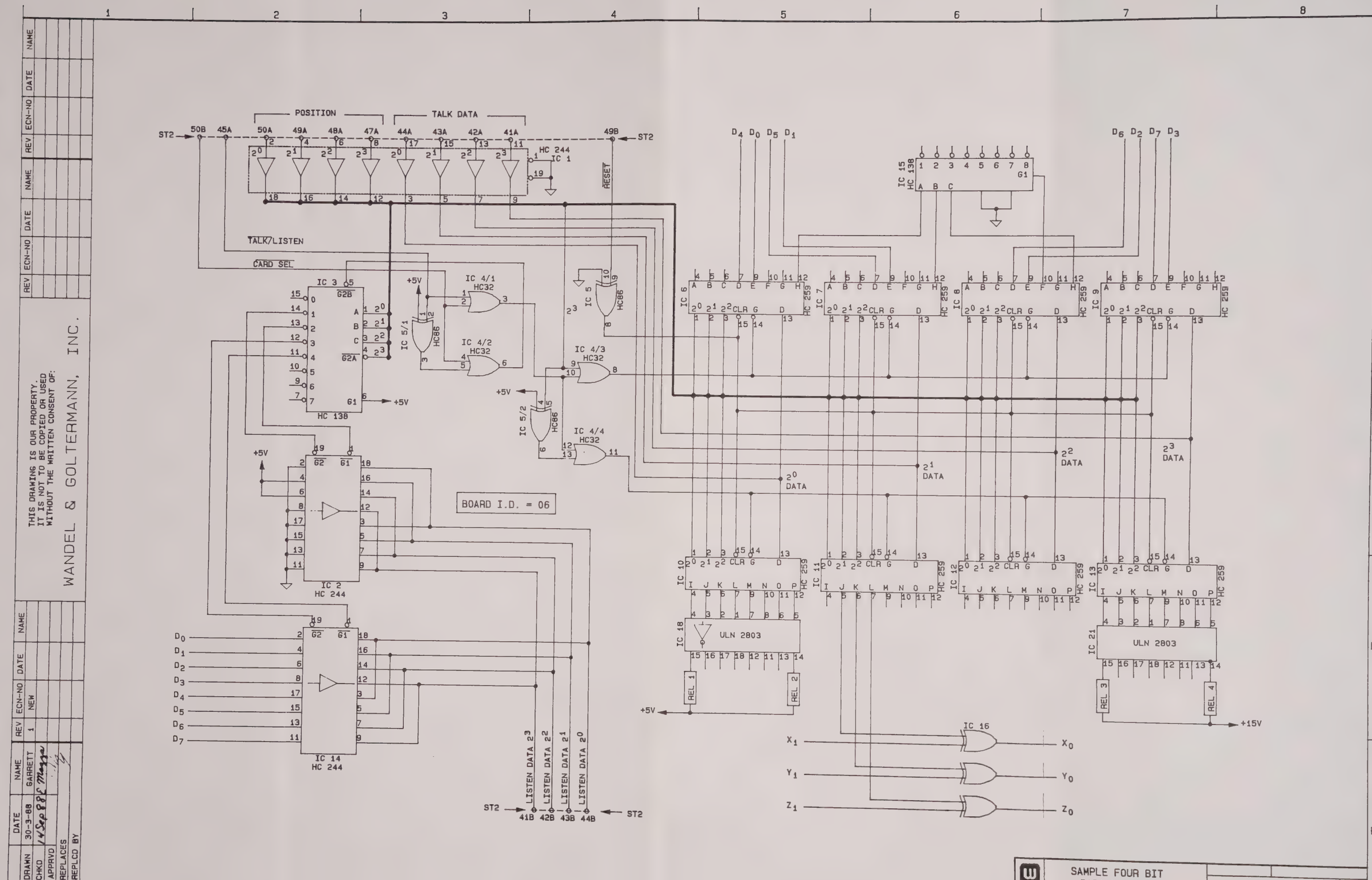
The information combination on these lines determines which element is written to or read from. The card select signal selects which module is being controlled. The $\overline{\text{Talk}}$/Listen signal determines whether the talk or listen circuitry is activated. The POS 2^3 signal selects between the addressable latches for positions A through H or I through P.

The $\overline{\text{CS}}$ (card select) input line must be low (0 volts) in order for any Four Bit Parallel Bus communication to occur between the system controller and the module. This line pulses low for each program data position. This signal is connected to IC 4/1 pin 2 and IC 4/2 pin 4 and will be used as talk or listen enable pulses depending on the $\overline{\text{Talk}}$/Listen input status.

The $\overline{\text{Talk}}$/Listen line is low when the bus is in talk (write) mode and high when the bus is in listen (interrogate) mode. When the bus is in talk mode, the low at IC 4/1 pin 1 will cause the low card select pulses to pass to output pin 3. The low pulses at this point enable the talk circuitry. When the bus is in listen mode, the low at IC 4/2 pin 5 will cause the low card select pulses to pass to output pin 6. The low pulses at this point enable the listen circuitry.

The status of position line POS 2^3 selects between positions A through H of IC 6 through IC 9 and I through P of IC 10 through IC 13. When the POS 2^3 line is inactive and low, a low at IC 4/3 pin 9 causes the low talk enable pulses at pin 10 to be passed to output pin 8. This will enable the parallel latches for data positions A through H. When the POS 2^3 line is active and high, the low at IC 4/4 pin 13 causes the low talk enable pulses at pin 12 to be passed to output pin 11. This will enable the parallel latches for data positions I through P. The talk data can now be latched through the appropriate addressable parallel latches.


ST2
TALK
44A
43A
42A
41A
2^0
2^1
2^2
2^3
IC 3
74LS259
IC 4
74LS259
IC 5
74LS259
IC 6
74LS259
74LS86
IC2/1
IC2/4
IC2/2
48A
POS 2^2
49A
POS 2^1
50A
POS 2^0
49B
RESET
74LS32
IC1/1
IC1/3
IC1/2
45A
T/L
50B
47A
CS
POS 2^3
1B
ST2
ST1
R1
3R3
1mH
+5V
C2
47µF
C1
6.8µF
15A, 15B
19A, 19B, 20A
ST1
THIS DRAWING IS OUR PROPERTY.
IT IS NOT TO BE COPIED OR USED
WITHOUT THE WRITTEN CONSENT OF:
WANDEL & GOLTERMANN, INC.
DRAWN 14-JUL-88 MANRIQUEZ
CHKD 14 July 88
APPRVD
REPLACES
REPLCD BY
REV 1 ECN-NO NEW DATE 14JUL88 NAME MRM
SAMPLE FOUR BIT PARALLEL
BUS INTERFACING CIRCUITRY
SERIES A
FIGURE 4.3.4
PG 1
OF 1



THIS DRAWING IS OUR PROPERTY. IT IS NOT TO BE COPIED OR USED WITHOUT THE WRITTEN CONSENT OF:

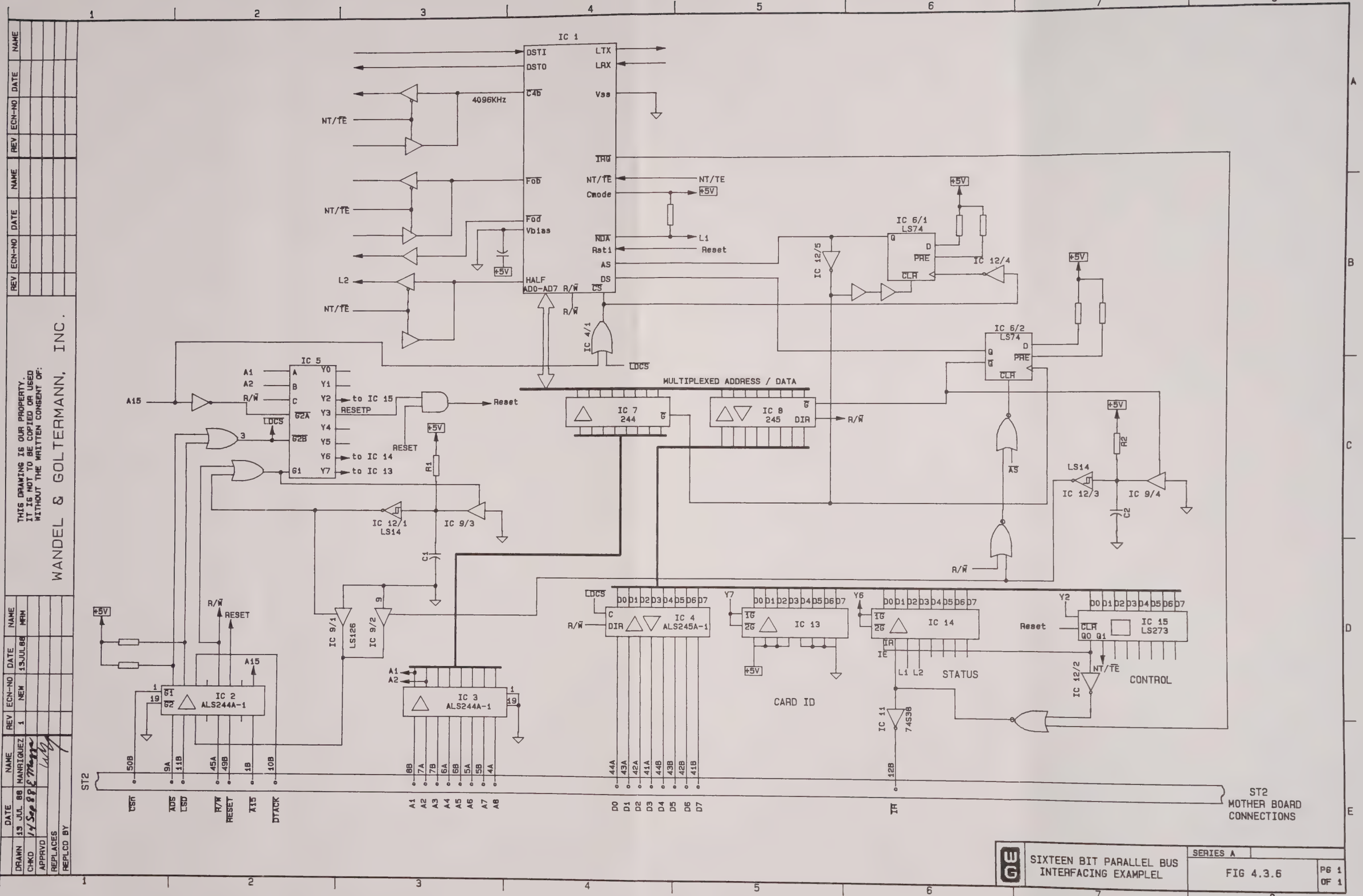
WANDEL & GOLTERMANN, INC.

	DATE	NAME	REV	ECN-NO	DATE	NAME
DRAWN	30-3-88	GARRETT	1	NEW		
CHKD	14 Sep 88	Maggie				
APPRVD						
REPLACES						
REPLCD BY						

SAMPLE FOUR BIT PARALLEL BUS CIRCUITRY

FIGURE 4.3.5

PG 1 OF 1



THIS DRAWING IS OUR PROPERTY. IT IS NOT TO BE COPIED OR USED WITHOUT THE WRITTEN CONSENT OF:

WANDEL & GOLTERMANN, INC.

	NAME	DATE	ECN-NO	REV
DRAWN	MANRIQUEZ	13 JUL 88		
CHKD		14 Sep 88		
APPRVD				
REPLACES				
REPLCD BY				

	NAME	DATE	ECN-NO	REV
	MRM	13JUL88	NEW	1

SIXTEEN BIT PARALLEL BUS INTERFACING EXAMPLE1

SERIES A

FIG 4.3.6

PG 1 OF 1

4.3.5.2 Relationship Between Input Lines of the Parallel Latches (Talk Circuitry)

The information latched to the outputs of the addressable latch ICs depends on the information present at the position lines and the talk data lines when a card select pulse reaches the enable pins. The position lines are connected in parallel to all of the addressable latch ICs, and each of the talk data lines is connected to a different addressable latch. IC 6 and IC 10 latch the 2^0 talk data to the appropriate output pins; IC 7 and IC 11 latch the 2^1 talk data to the appropriate output pins; IC 8 and IC 12 latch the 2^2 talk data to the appropriate output pins; and IC 9 and IC 13 latch the 2^3 talk data to the appropriate output pins. The following chart shows the correlation between the code on the position lines and the output pin that the data is latched to.

Pos 2^0	Pos 2^1	Pos 2^2	Pos 2^3	Address
0	0	0	0	A
1	0	0	0	B
0	1	0	0	C
1	1	0	0	D
0	0	1	0	E
1	0	1	0	F
0	1	1	0	G
1	1	1	0	H
0	0	0	1	I
1	0	0	1	J
0	1	0	1	K
1	1	0	1	L
0	0	1	1	M
1	0	1	1	N
0	1	1	1	O
1	1	1	1	P

4.3.5.3 Listen Circuitry

The information to be read by the controller is gated one position at a time to the Listen Data lines. IC 3 is used as a position decoder. The listen enable pulses trigger IC 3 for each position that is to be read. The position information selects one of the outputs A through H. If positions I through P are needed, another position decoder could be used that would be active when POS 2^3 is high and the listen enable pulse is low. The output of the position decoder is a negative pulse and triggers the proper information to the Listen Data lines.

4.3.5.4 Examples of Using the Talk Circuitry

The output pins of the addressable parallel latches, ICs 6 through 13, form the interface between the Four Bit Parallel Bus and the controllable elements. The examples of circuitry given below illustrate the utilization of the bus.

The D and E outputs of IC 6 through IC 9 are connected to an eight bit parallel bus. The four least significant bits, D_0 through D_3, derive their states from the "E" outputs of the latch ICs, while D_4 through D_7 are controlled by the "D" outputs. For example, in order to latch "01001100" on the bus, send the write string "W1DE4<" where D = "0100" (decimal value is 4) and E = "1100" (decimal value is 12 and ASCII character is "<").

IC 15 is a demultiplexer and is connected to the "H" outputs of IC 6 through IC 8. This illustrates further decoding of the Four Bit Parallel Bus. The three latched lines are used to

select one of the eight output lines of IC 15. An additional connection is also used from the "F" output of IC 8. This is used to enable IC 15.

Relay control is another common use for the Four Bit Parallel Bus. Two driver ICs, IC 18 and IC 21 are connected to the latched lines of IC 13 and IC 15 respectively. These open collector inverters have high drive capability for powering relay coils.

IC 16 shows a very simple example of combinational logic controlled by the Four Bit Parallel Bus. The system controller sends data to the Exclusive ORs. When a high is sent from the latches to the inputs of IC 16, the data on lines X_1, Y_1, and Z_1 will be inverted. When a low is sent from the latches to the inputs of IC 16, the data on lines X_1, Y_1, and Z_1 will not be inverted.

4.3.5.5 Examples of Reading Data Back to the Controller

Assume the UTI-1 module contains an eight bit data bus D_0 through D_7. As shown, these lines are connected to IC 14. Reading these lines is a simple matter of sending the command to read position "D" and "E". Selection of position "D" brings pin 19 of IC 14 low and places D_4 through D_7 on the Listen lines, while selection of position "E" brings pin 1 of IC 14 low and places D_0 through D_3 on the Listen lines.

A hardwired board identification code is highly desireable on all UTI-1 modules. This allows a software routine to determine what type of module is installed in each motherboard slot. IC 2 shows how this board ID can be implemented using the Listen lines. In this example, the ID is the hexadecimal value "06". The read string "I1BC" reads "B" first by bringing pin 1 of IC 2 low, enabling the four gates with outputs at pins 3, 5, 7, and 9. Since their respective inputs are all grounded, all four Listen lines will have a 0 state. When position "C" is called, the other four gates of IC 2 output to the Listen lines by bringing pin 19 of IC 2 low. Their input states are "0110", indicating the value "6".

4.3.6 Sample Sixteen Bit Parallel Bus Interfacing Circuitry

Unlike the Four Bit Parallel Bus, the Sixteen Bit Parallel Bus can be interfaced to intelligent devices with a microprocessor interface; therefore, the exact interface circuitry will depend upon factors such as data width of the device, number of addresses, if the address and data lines are multiplexed or not, and the timing specified at the microprocessor interface.

Figure 4.3.6 shows a sample circuit which demonstrates the interfacing concepts of a UTI-1 module to the Sixteen Bit Parallel Bus. This circuit interfaces a Mitel MT8930 Subscriber Network Interface chip for ISDN to the parallel bus. The MT8930 has a eight bit multiplexed address/data microprocessor interface.

IC2 buffers the Address strobe $\overline{ADS}$, the data strobe $\overline{LDS}$, and the Read/Write signal R/$\overline{W}$. IC2 is enabled by the $\overline{CSn}$ ($\overline{Card\ Select}$) line from the UTI-1 motherboard. When the $\overline{CSn}$ line is high, IC2 is tristated and the $\overline{ADS}$ and $\overline{LDS}$ line on the module are pulled up; therefore, the UTI-1 module is not affected by any activity of the parallel bus on the motherboard. To perform a Read or Write access to the UTI-1 module, the Parallel Bus Interface module has to be programmed to select this UTI-1 module by pulling the corresponding $\overline{CSn}$ line low.

IC3 is a 74LS244 buffer used to receive the address lines A_1 to A_8 from the UTI-1 motherboard. IC4 transfers the data lines D_0 to D_7 in both directions. All devices in this circuit are connected to the lower data byte D_0 to D_7 of the Sixteen Bit Parallel Bus. The upper data bits D_8 to D_{15} are not used. The devices connected to the 8 bit data bus on the

UTI-1 module are the MT8930 IC1, the Card ID register IC13, control register IC15, and the status register IC14.

IC5 is a 74LS138 3:8 decoder. Select input line C of IC5 is connected to R/$\overline{W}$. This allows four decoder outputs to be used for write acceses and four decoder outputs to be used for read accesses. In this design only the standard UTI-1 module registers are implemented. The user is free to use additional read or write registers if required. The address of standard UTI-1 module registers is defined in section 3.4.5.

When accessing any of the standard UTI-1 module registers, address line A_{15} is high; therefore $\overline{G2A}$ of IC 5 is enabled. $\overline{G2B}$ of IC5 is enabled when $\overline{ADS}$ and $\overline{LDS}$ are low at the beginning of the cycle. The $\overline{DTACK}$ signal is asserted after the delay provided by the RC network R1 and C1. (IC12 is a LS14 buffer with hysterisis input.) The delay is needed to provide the propogation delay of IC5 and to allow for the data to settle before being read by the system controller or written to a register.

For write access pin G1 of IC5 is disabled when $\overline{DTACK}$ is asserted, this produces a rising edge on the decoded Y output causing the data to be latched into the selected write register. For read cycle the decoder IC5 remains enabled until the end of the cycle. (i.e. when the Parallel Bus Interface Module releases the address or data strobes.) This causes the selected read register to drive the data bus until the system controller has accepted the data.

The UTI-1 module ID is hard wired to the inputs of the card ID register (IC13). IC14 is the status register and IC 15 is a 74LS273 octal latch used as the control register. Bit 0 and 1 of the status register and bit 0 of the control register are used as defined by section 3.4.5 (Standard UTI-1 module registers). Writing a 1 to bit 0 of the control register enables interrupts from the MT8930. Bit 1 of the status register can be polled by the software to determine if this module is requesting an interrupt service. The MT8930 removes the interrupt request when its interrupt register is read. IC11 is an open collector driver for the interrupt line $\overline{IR}$ on the motherboard.

Bits 2 to 7 of the status register can be user defined. In this circuit bit 2 is connected to the status output NCA of the MT8930. Bit 3 is connected to the status output $\overline{HALF}$ of the MT8930. These status outputs are used to determine the current state of the MT8930.

Bits 1 to 7 of the control register can be user defined. In this circuit Bit 1 is used to control the mode of the MT8930 to NT (Network Termination) or TE (Terminal Equipment).

The UTI-1 module can be reset either by a write to relative address FFFF or if the reset line on the UTI-1 motherboard is pulsed. The Y_3 output of IC5 is pulsed when any data is written to relative address FFFF (Reset Register). This causes the UTI-1 module to be reset. This method for resetting must be used only if individual modules must be reset. The Parallel Bus Interface Module can be programmed to pulse the RESET line on the motherboard this causes all the modules to be reset. Note that the effect of a reset on the module depends upon the design of the module.

The MT8930 has an eight bit multiplexed address/data microprocessor interface. IC7 and IC8 are used to multiplex the address and data lines to the AD_0 to AD_7 pins of the MT8930.

The A_{15} address line is used to enable the chip select input $\overline{CS}$ of the MT8930. This causes the MT8930 to be selected for all accesses where the address bit A_{15} is 0. At the beginning of an access cycle to the MT8930, the $\overline{CS}$ input of the MT8930 goes low. IC6/1 is a D flip-flop used as a monoshot. It generates a high going pulse which is applied to the address strobe input AS of the MT8930 and also enables IC7 which drives the address lines to the multiplexed AD_0 to AD_7 pins of the MT8930. The MT8930 latches the address

on the falling edge of the AS pulse. Next, IC6/2 enables the data transceiver IC8 and applies a pulse to the data strobe input DS of the MT8930 which connects the AD_0 to AD_7 pins to the DATA bus allowing the data to be written into or read from the MT8930. For write access, the data pulse to the DS input of MT8930 is cleared when the $\overline{DTACK}$ signal is asserted for read access, the Data pulse is applied until the system controller reads the data from the MT8930 and clears the address strobe signal at the end of the cycle. The RC network R2 and C2 provides a delay so the data settles before asserting the $\overline{DTACK}$.

IC9/1 and IC9/2 are used to logically OR the $\overline{DTACK}$ signals generated by the interface circuitry for the MT8930 and for the standard UTI-1 registers.

The above description gives an example of interfacing an intelligent device and Read/Write registers to the parallel bus. It is the designers responsibility to ensure that the interface circuitry meets all the specifications of the device and the parallel bus.

4.3.7 Cable Shielding

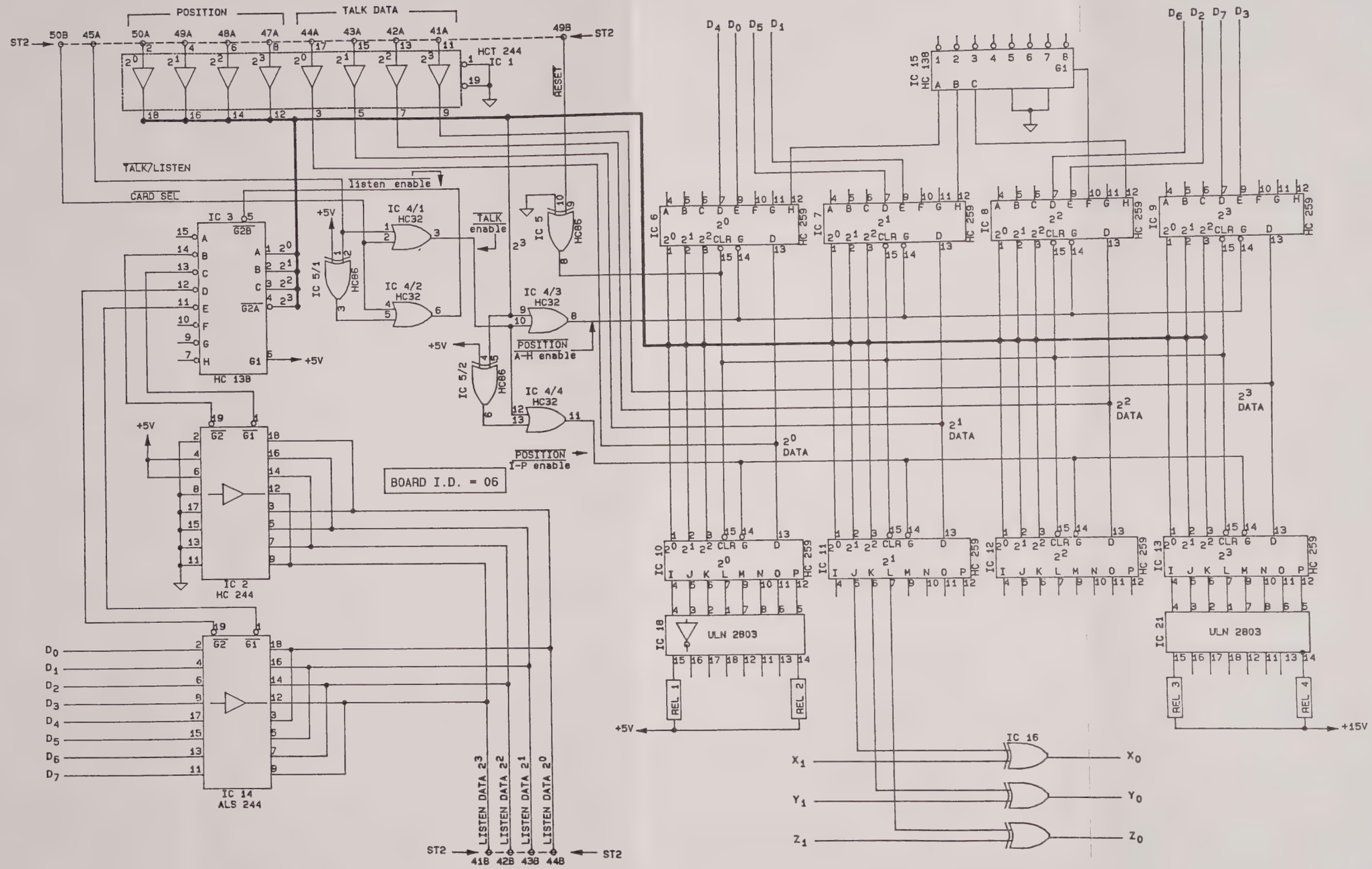
All cables connected to the UTI-1 and to the modules must be shielded. Shielding provides the necessary electromagnetic protection between signal wires and suppresses undesired noise from adjacent conductors or wires. Another purpose of cable shielding is to prevent signals from being radiated into the atmosphere. This shield must be connected to chassis ground on each end of the cable.

4.3.8 Module Identification Numbers

A module identification number has been assigned to all standard modules. These numbers are read back in hex. See the description of the 4 Bit Parallel Bus or the 16 Bit Parallel Bus for examples of how this is accomplished.

The hex numbers 01 (decimal equivalent is 01) through DF (decimal equivalent: 223) are reserved for standard modules supplied by Wandel & Goltermann. The hex numbers E0 (decimal equivalent: 224) through FE (decimal equivalent: 254) have been set aside for custom modules. If an attempt is made to read the ID number from a vacant slot, the hex number FF (decimal equivalent: 255) will be read by the controller; this ID number should not be used in the design of any module.

See the IEEE Interface module BN 9537/00.01 or the Parallel Bus Interface module BN 9537/00.27 programming sections for information on reading back the identification number.



THIS DRAWING IS OUR PROPERTY.
IT IS NOT TO BE COPIED OR USED
WITHOUT THE WRITTEN CONSENT OF:
WANDEL & GOLTERMANN, INC.

	NAME	DATE	ECN-NO	REV
DRAWN	GARRETT	30-3-88	NEW	1
CHKD		11 May 88		
APPRVD				

REPLACES

REPLCD BY

SAMPLE FOUR BIT PARALLEL BUS CIRCUITRY

FIGURE 4.3

PG 1 OF 1

5. Interchangeable Test Adapter (ITA) Design Guidelines

Contents **Page**

5.1. Physical Guidelines 5.1-1

5.2. Standard Mechanical Parts 5.2-1

5.3. Electrical Guidelines 5.3-1
- 5.3.1 +5V, +15V, and -15V Power Limitations 5.3-1
- 5.3.2 Test Stimulus to the Unit Under Test 5.3-4
- 5.3.3 Controlling the Interchangeable Test Adapter 5.3-4
- 5.3.4 Signal Loading and Drive Requirements 5.3-5
- 5.3.5 Interchangeable Test Adapter Identification Number 5.3-5

5. Interchangeable Test Adapter (ITA) Design Guidelines

With the aid of this section, an experienced hardware designer can design custom personality circuits for the Interchangeable Test Adapter. For proper operation of this circuit, great care must be taken to conform to both the physical and electrical specifications.

5.1. Physical Guidelines

The physical dimensions of any ITA personality module are extremely important. The module must be correctly fitted to insure proper electrical connections to the connectors on the UTI-1 modules.

See figure 5.1. for the recommended dimensions. Section 5.2. of this manual contains some of the standard mechanical parts necessary.

Notes: for Figure 5.1.

1) All tolerances are 0.25mm unless otherwise specified.
2) Tolerances are non-accumulative on linear dimensions.
3) Solder mask both sides using DEXTER HYSOL 1000, PC-401 or equivalent over bare copper.
4) Dashed line to edge of board indicates "keep out" area for components and NCS traces, except digital grounds.
5) Place only required connector pins and 2 clearance holes for each connector used.
6) Provide approximately 1/2" x 1" solder mask relief around all 12 mounting holes. These mounting holes should be connected to digital ground.
7) Use SMOBC if NCS has very wide traces.

Terminology

CS	Component side of PC board.
NCS	Non-component side of PC board.

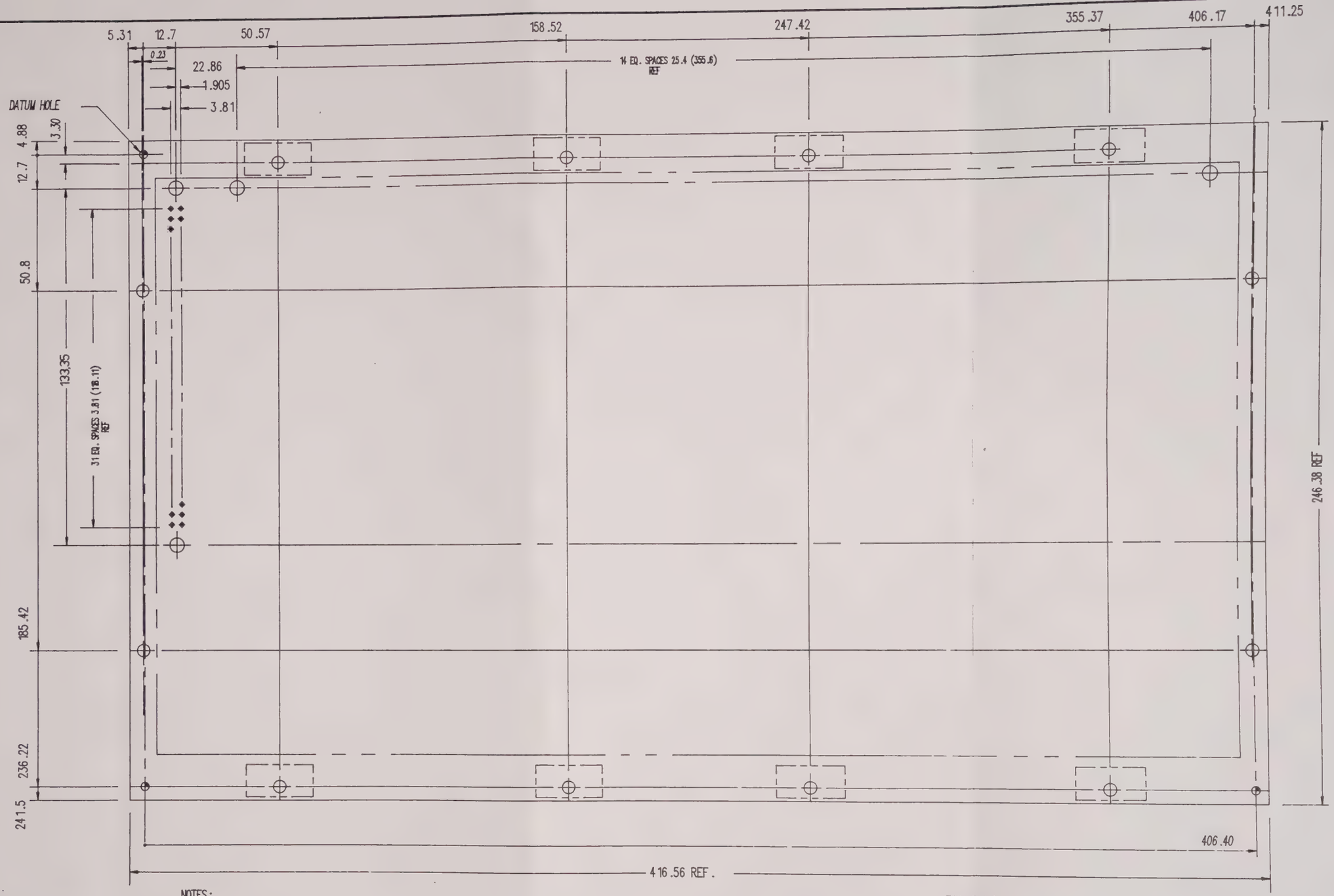


FIG: 5.1.0

NOTES:

1. Soldermask both sides using DEXTER HYSOL 1000, PC-401 or equiv. OVER BARE COPPER.
2. Dashed line to edge of board indicates keep-out area for comp. and NCS traces, except digital gnd.
3. Place only req'd. conn. pins & 2 clearance holes for each conn. used. Comp. and traces, may be placed around those positions. Number each connector and pin position used as necessary.
4. Provide approx. 1/2" x 1" solder mask relief around all 12 mounting holes. These mounting holes shall be connected to digital ground.

⊕ ø 4,76 (After plating)
⊕ ø 3,175 (Non-plated thru)
⊕ ø 5,56 (Non-plated thru)
✦ ø 1,20 (After plating)

Oberfläche/Finish:

Ausg. Issue	Änderung Change	Tag Date	Name
1	—	12.4.88	L.K.H.

Darstellung Methode E
First Angle Projection

	Tag Date	Name
Bearb. Drawn	21/3/88	D. Beard
Gepr. Check		

WANDEL & GOLTERMANN, INC.
Electronic Measurement Technology
Research Triangle Park, North Carolina

Halbzeug und Werkstoffe/Material
FR4 glass epoxy, 1oz. copper both sides B-stage FR4-116
1,58mm thick

Benennung/Designation
MASTER FOR ITA
MOUNTED PERS. BD.

9538-FIG: 5.1.0

Ersatz für/Replaces:

Winkelmasse/Ang. Tol.:

Allgemeintoleranzen/Std. Tol.

Required	Nennmaßbereich/Millimeters 1 bis 6	über 6 bis 30	über 30 bis 100	über 100 bis 300	über 300 bis 1000
X	±0.05	±0.1	±0.15	±0.2	±0.3
X	±0.1	±0.2	±0.3	±0.5	±0.8
	±	±	±	±	±

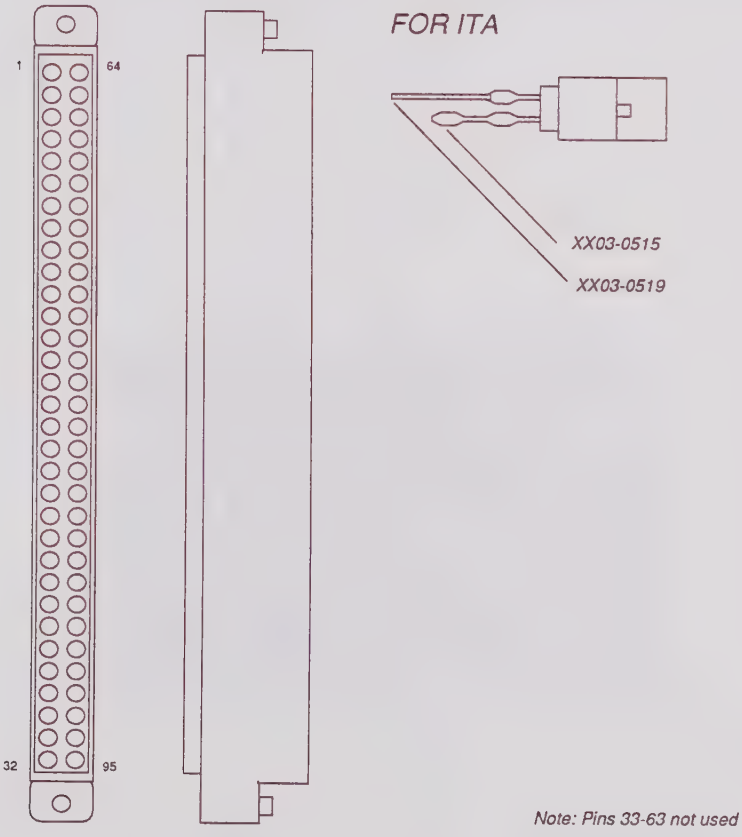
Verteiler Distribution

Massstab Scale 1/1

Page 1 Of 1

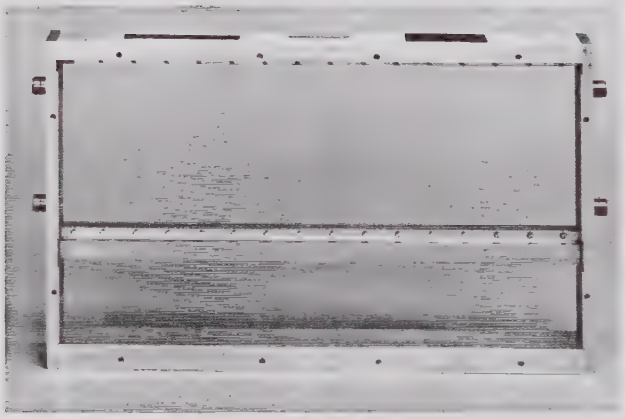
5.2. Standard Mechanical Parts

Part Number	Description	Notes
XX20-0136.00	Test fixture connector frame	
XX05-0015.00	Screw, cylinder, slot M4x8	For mounting board on ITA
XX05-0205.00	Washer, flat, for M4	For mounting board on ITA
XX03-0511.00	Connector W/O pins,64 pin	
XX03-0515.00	Pin, malecrimp	
XX03-0519.00	Pin, maleinsert	with wire wrap post, 44mm

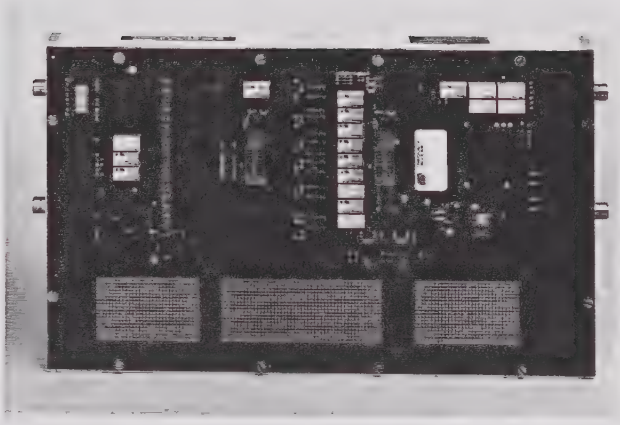


Note: Pins 33-63 not used

Figure 5.2. 64 pin connector details



Interchangeable Test Adapter (ITA)



ITA Based Personality Board for
customized circuitry and Pin-Electronics Testing

ITA/IC Socket Fixture

From ITA Frame to ITA/Test Fixture

5.3. Electrical Guidelines

5.3.1 +5V, +15V, and -15V Power Limitations

When designing an ITA personality board, the combined output power of the modules and the board must not exceed the maximum allowed value, and the +5V, -15V, and +15V individual power ratings must not be exceeded.

Refer to the Standard Module Power Consumption table in this section to insure that power consumption limits are not exceeded.

The motherboard provides +5, +15, and -15 volt connections to the Standard Latch Module BN 9537/00.24. This module in turn connects the voltages to the Interchangeable Test Adapter through its Bu 1 connector.

Motherboard Power for Modules (Series A - C)

Voltage	Current (Amps)	Power (Watts)
+5	1 to 11	55
+15	0 to 1	15
-15	0 to 1	15

*Total power not to exceed 75 Watts

Motherboard Power for Modules (Series D...)

Voltage	Current (Amps)	Power (Watts)
+5	0 to 15	75
+15	0 to 4	60
-15	0 to 4	60

* Total Power not to exceed 175 Watts

Power through Standard Latch Module for Interchangeable Test Adapter

Voltage	Current (Amps)	Power (Watts)
+5	0 to 15	10
+15	0 to 4	4.5
-15	0 to 4	4.5

Standard Module Power Consumption in Watts

Standard Module	+5 Volts	+15 Volts	-15Volts	Total	Notes
9537/00.01 IEEE-488 Int.	8.75		-----	8.75	
9537/00.02 Digital Int.	9.50	-----	-----	9.50	
9537/00.03 Analog Module	6.50 3.00 17.50	0.20 0.20 0.20	0.20 0.20 0.20	6.50 5.90 17.90	1 2 3
9537/00.04 6 × 8 Switch Matrix	6.00 3.75 25.00	----- ----- -----	----- ----- -----	6.00 3.75 25.00	1 2 3
9537/00.06 Custom Termination Module	8.00 5.00 25.00	----- ----- -----	----- ----- -----	8.00 5.00 25.00	1 2 3
9537/00.23 2 × 32 Switch Matrix	5.00 2.50 38.75	----- ----- -----	----- ----- -----	5.00 2.50 38.75	1 2 3
9537/00.24 Standard Latch Module	12.50 4.50 23.75	0.75 0.75 0.75	1.50 1.50 1.50	14.75 6.75 26.00	1 2 3
9537/00.25 Oscilloscope Probe Access Module	2.50 1.50 19.00	2.00 2.00 2.00	0.50 0.50 0.50	5.00 4.00 21.50	1 2 3
9537/00.27 Parallel Bus Ex	8.00	-----	-----	8.00	

Be sure to take into account the power consumption of all modules and the Personality Based Interchangeable Test Adapter.

Notes:

1. Power consumption during normal usage. This power rating should be used in most cases.
2. Power consumption during minimal usage. This power rating should be used when more than one module is used and this is the secondary module or if this module is not fully utilized.
3. Maximum possible power consumption. This condition is not typical, but includes all relays energized and all components utilized under normal loads.

The conditions for the applicable modules under the above conditions are described in the following table.

Analog Module BN 9537/00.03

1. DMM (Bu5), Tx (Bu6), Rx (Bu7), Spare (Bu8), Spare (Bu9), and Spare (Bu10) are connected to the motherboard or Interchangeable Test Adapter. The Tx and Rx ports are set to the single ended mode. V1 through V4 and all Auxiliary Supply voltages are connected to the motherboard or Interchangeable Test Adapter. The AC and DC Auxiliary Supply Voltages are combined.
2. DMM (Bu5), Tx (Bu6), and Rx (Bu7) are connected to the motherboard or Interchangeable Test Adapter. The Tx and Rx ports are set to the balanced mode. V1 through V4 and all Auxiliary Supply voltages are connected to the motherboard or Interchangeable Test Adapter. The AC and DC Auxiliary Supply Voltages are combined.
3. All relays are energized.

6 × 8 Switching Matrix BN 9537/00.04

1. The six motherboard busses (AB1 through AB6) are connected to six of the Interchangeable Test Adapter output channels. The two remaining output channels are terminated.
2. All eight Interchangeable Test Adapter output channels are terminated.
3. All relays are energized.

Custom Termination Module BN 9537/00.06

1. Up to twenty relays are energized. This allows for different combinations of Programmable Decadic Impedances and Complex Impedances.
2. Up to twelve relays are energized. This will allow the connection of two complex impedances in series or parallel with a Programmable Decadic Impedance of no more then 6 relays.
3. All relays are energized.

2 × 32 Switch Matrix Module BN 9537/00.23

1. Two of the input channels from either the motherboard or rear panel are connected to two different Interchangeable Test Adapter output channels. Two additional output channels are terminated.
2. Two of the input channels from either the motherboard or rear panel are connected to two different Interchangeable Test Adapter output channels.
3. All relays are energized.

Standard Latch Module BN 9537/00.24

1. All of the latched talk lines and listen lines are connected to the Interchangeable Test Adapter.
2. Only the permanently connected 32 talk lines are connected to the Interchangeable Test Adapter.
3. All relays are energized.

Oscilloscope Probe Access Module BN 9537/00.25

1. One input channel is connected to Output A, and another input channel is connected to Output B. Both output channels are set to 100.
2. One input channel is connected to Output A, and another input channel is connected to Output B. Both output channels are left at the preset mode of 10.
3. All relays are energized.

5.3.2 Test Stimulus to the Unit Under Test

The primary purpose of the Interchangeable Test Adapter (ITA) is to provide the test stimulus and connect the measuring equipment to the Unit Under Test (UUT). The signals are connected to the ITA through the front connector (Bu 1) of the different interfacing modules located in the UTI-1.

Many different standard interfacing modules are available from Wandel & Goltermann. The Analog Module (BN 9537/00.03) is the basic module for interfacing analog signals and measuring equipment. This module can be expanded by using the 6×8 (9537/00.04) or 2×32 (BN 9537/00.23) switching matrixes. The Digital Interface module (BN 9537/00.01) is the basic module for interfacing digital signals. For more information on these and other available modules, see their individual descriptions.

Custom modules can also be designed and built to meet customer needs. See section 4 for design guidelines.

5.3.3 Controlling the Interchangeable Test Adapter (ITA)

The UTI-1 has a 4 or 16 bit parallel bus available for controlling the UTI-1 boards. Of these two busses, the IEEE-488 Interface Module supports only the Four Bit Parallel Bus, while the Parallel Bus Interface Module supports both the Four Bit Parallel Bus and the Sixteen Bit Parallel Bus.

The Four Bit Parallel Bus does not connect directly to the ITA. However, the parallel bus information to and from the ITA can be latched by the Standard Latch Module (BN 9537/00.24). This module has BCD parallel lines to the ITA capable of latching information from the Four Bit Parallel Bus. This information is then provided to control elements, such as relays and read lines, which are capable of transferring information from BCD parallel lines to the Four Bit Parallel Bus. For more information on the use and operation of the Standard Latch Module, see the description of this module.

The Sixteen Bit Parallel Bus from the Parallel Bus Interface Module connects directly to the ITA through its Bu 1 connector. If this bus is used by the personality board, the bus interfacing circuitry must be included on this circuit. The Sixteen Bit Parallel Bus is useful when a microprocessor or a peripheral is required on the personality board. For more information on the operation and applications of this bus, see the Sixteen Bit Parallel Bus and Parallel Bus Interface Module sections.

5.3.4 Signal Loading and Drive Requirements

The following signal loading and drive guidelines must be met to ensure reliable data transfers and operation of the Standard Latch Module.

Standard Latch Module BN 9537/00.24 Receiver and Driver Requirements

The maximum loadings on the talk lines should be 10 LS loads. The listen lines should be driven by TTL compatible outputs.

16 Bit Parallel Bus Receiver and Driver Requirements

Signal Name	Max. Recvr. Loading	Suggested Receiver	Suggested Driver
A_1 - A_{15} $\overline{UDS}$, $\overline{LDS}$ $\overline{RESET}$, R/$\overline{W}$ 74LS241	10 74LS load	74LS244, 74LS245, 74LS240,	
D_0 - D_{15}	10 74LS load	74LS245, 74LS244, 74LS645,	74LS245, 74LS244, 74LS645
$\overline{DTACK}$, $\overline{IR}$ TRIG1, TRIG2			74LS245, 74LS244, 74LS645

5.3.5 Interchangeable Test Adapter Identification Numbers

A test adapter identification number has been assigned to all adaptors supplied by Wandel & Goltermann. These numbers are read back in hex. See the description of the 4 Bit Parallel Bus or the 16 Bit Parallel Bus for examples of how this is accomplished.

The hex numbers 01 (decimal equivalent is 01) through DF (decimal equivalent: 223) are reserved for standard modules supplied by Wandel & Goltermann. The hex numbers E0 (decimal equivalent: 224) through FE (decimal equivalent: 254) have been set aside for custom modules. If an attempt is made to read the ID number from a vacant slot, the hex number FF (decimal equivalent: 255) will be read by the controller; this ID number should not be used in the design of any module.

See the IEEE Interface module BN 9537/00.01 or the Parallel Bus Interface module BN 9537/00.27 programming sections for information on reading back the identification number.

Contents

Page

1. Introduction 1-1
2. Specifications 2-1
   - 2.1. DC Characteristics 2-1
   - 2.2. ITA Relay Driver Characteristics 2-1
   - 2.3. Data Transmission Sequence 2-1
   - 2.4. Signal Load and Drive Requirements 2-3
3. Operating Description 3-1
   - 3.1. Detailed Description of Features 3-1
     - 3.1.1 Computer Control 3-1
     - 3.1.2 Control of UTI-1 Modules 3-2
     - 3.1.3 Interchangeable Test Adapter (ITA) Control 3-2
     - 3.1.4 ITA Identification Number 3-2
     - 3.1.5 Mechanical Start Switch 3-2
     - 3.1.6 External Instrument Control 3-2
   - 3.2. Programming 3-3
     - 3.2.1 Writing to Devices on the Four Bit Parallel Bus 3-3
     - 3.2.2 Reading from Devices on the Four Bit Parallel Bus 3-4
     - 3.2.3 Programming Internal Functions 3-5
       - 3.2.3.1 Programming Start Switches 3-6
       - 3.2.3.2 Programming Relay Drivers 3-7
       - 3.2.3.3 Reading the Status of the Listen Lines from the ITA 3-8
       - 3.2.3.4 Reading the ITA Identification Number 3-9
     - 3.2.4 Controlling the UTI-1 Modules 3-10
     - 3.2.5 Reading from the UTI-1 Modules 3-12
     - 3.2.6 Writing to Buffer Stores 3-13
     - 3.2.7 Reading from Buffer Stores 3-15
   - 3.3. Circuit Description 3-17
     - 3.3.1 Microprocessor Interface Circuitry 3-17
     - 3.3.2 Four Bit Parallel Bus Architecture on the UTI-1 Motherboard 3-19
     - 3.3.3 Control of UTI-1 Modules 3-22
       - 3.3.3.1 Writing to UTI-1 Modules 3-23
       - 3.3.3.2 Interrogating UTI-1 Modules 3-24
     - 3.3.4 ITA Circuitry Connections 3-26
     - 3.3.5 Mechanical Switch Activation 3-28
     - 3.3.6 Four Bit Parallel Bus Architecture on the Control Expansion Connector 3-29
     - 3.3.7 Controlling Instruments on the Control Expansion Connector 3-31
       - 3.3.7.1 Writing to Instruments on the Control Expansion Connector 3-32
       - 3.3.7.2 Interrogating Instruments on the Control Expansion Connector 3-33

3.3.8 IEEE-488 Bus Address Switch 3-34
3.3.9 Monitor LEDs 3-35
3.4. Schematic Diagram / Parts List 3-37

IEEE-488 Interface Module Description and Operation

1. Introduction

The IEEE-488 Interface Module is used to transfer and convert data from the IEEE-488 format (specified in the IEEE-488 1975/1978 standards and the IEEE-488A 1980 Supplement) to the Four Bit Parallel Bus format used in the UTI-1 Universal Test Interface.

The Four Bit Parallel Bus can be used to control UTI-1 modules, external instruments with parallel BCD interfaces, and the personality circuit on the Interchangeable Test Adapter (ITA).

2. Specifications

2.1. DC Characteristics

Maximum power consumption

	+5V	+15V	-15V	Total
Current (Amps)	1.75	-----	-----	-----
Power (Watts)	8.75	-----	-----	8.75

Maximum power consumption of the external control expansion connector (+15Volts) ... 30 watts.

2.2. ITA Relay Driver Characteristics

Collector Current (Ic) . . . . . 350 mA
Collector Voltage (Vc) . . . . . 50 Volts
Saturation Voltage (Vcesat) . . . . . 1.6 Volt

2.3. Data Transmission Sequence

The following timing parameters apply to WRITE control blocks and INTERROGATE control blocks used in the Four Bit Parallel Bus and refer to wave forms shown in figures 2.3.a and 2.3.b.

Parameter Name		Min.	Max.	Unit
Address Pulse Width	(tAW)	80	120	µSec
Address Enable Delay	(tAE)	40	80	µSec
Address Enable Hold	(tAD)	20	150	nSec
Card Select Delay	(tSE)	2	2.5	µSec
Card Select Width	(tSW)	80	120	µSec

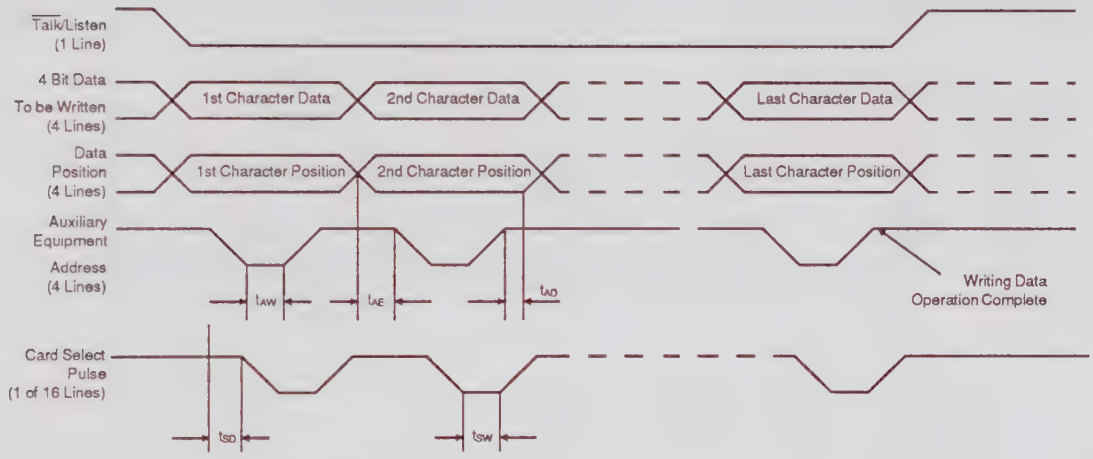


Figure 2.3.a Writing data to a device (Write control blocks)

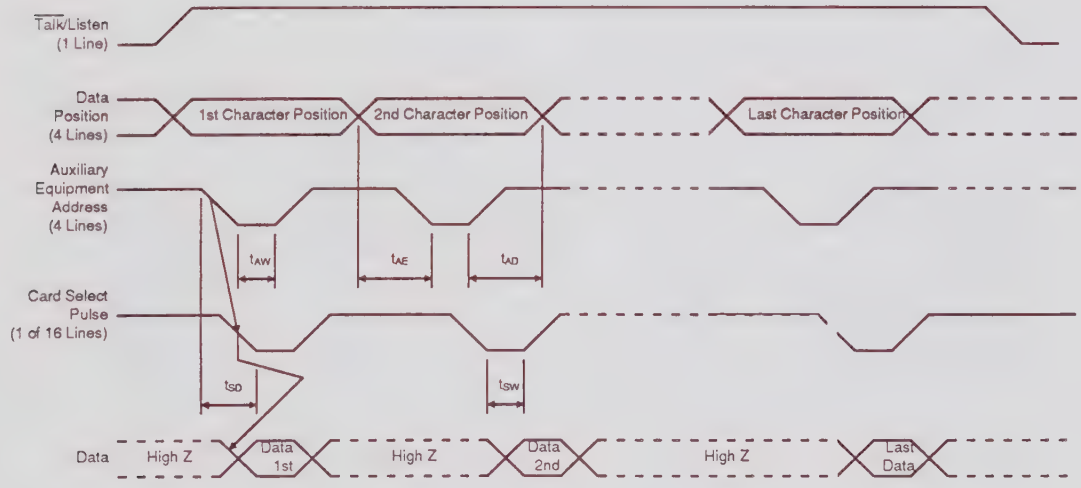


Figure 2.3.b Reading data from a device (INTERROGATE control block)

2.4. Signal Load and Drive Requirements

The following signal loading and drive guidelines must be met. This will help ensure reliable data transfers on the Four Bit Parallel Bus.

Do not terminate any signal line. All lines are terminated in the UTI-1 Motherboard.

Printed circuit card trace length for each signal should be kept shorter than three inches. Traces should be narrow and placed as far as possible from power and ground planes.

Table 2.4. Signal Load and Drive Requirements

Signal Name	Min. Recvr. Loading	Suggested Receiver	Suggested Driver	Note
TALK	1 74LS load	74LS240, 74LS241, 74LS244		
LISTEN			74ALS245A-1, 74ALS244A-1, 74ALS645A-1	1
POSITION 74LS241, 74LS244	174LS load	74LS240,		
CARD SELECT $\overline{CS_1}$ - $\overline{CS_{15}}$	1 74LS load	74LS240, 74LS241, 74LS244		2
$\overline{RESET}$	1 74LS load	74LS240, 74LS241, 74LS244		2
$\overline{T}$/L	1 74LS load	74LS240, 74LS241, 74LS244		
$\overline{REM}$/LOCAL	1 74LS load	74LS240, 74LS241, 74LS244		3
ADDR	1 74LS load	74LS240, 74LS241, 74LS244		3

Notes:

1. LISTEN lines must be enabled by the selected module during INTERROGATE control blocks only. Otherwise, these lines must be tristated.
2. These lines are unique to the UTI-1 Motherboard.
3. These lines are unique to Control Expansion Connector BU2.

3. Operating Description

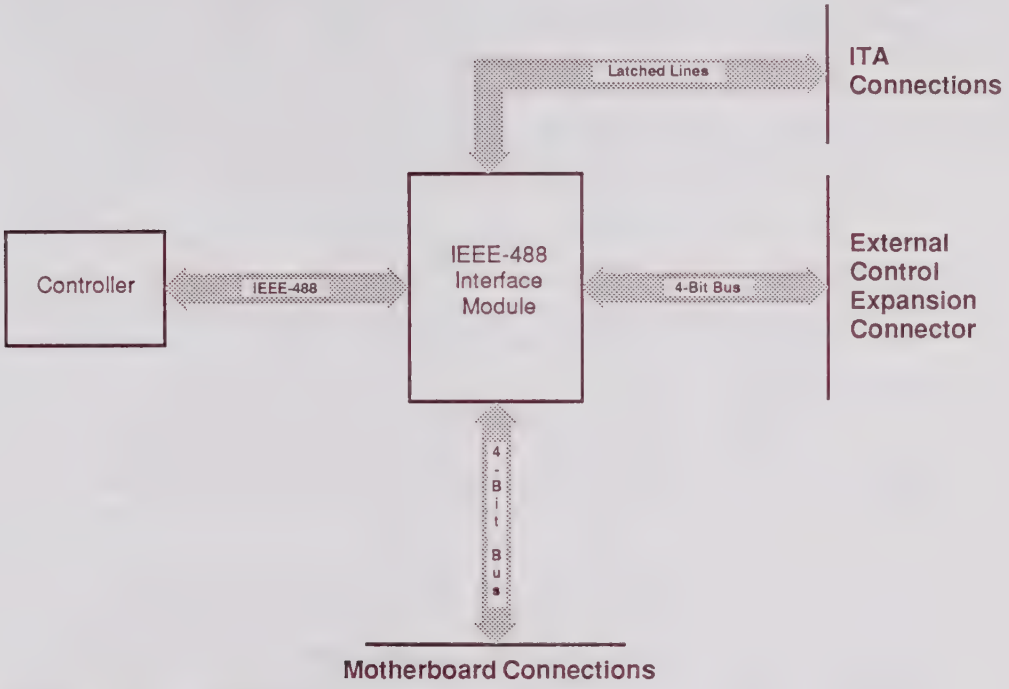


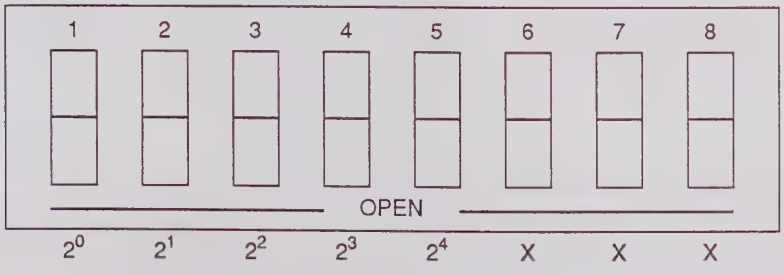
Figure 3. IEEE-488 Interface Module Block Diagram

3.1. Detailed Description of Features

3.1.1 Computer Control

The IEEE-488 Interface Module allows any computer equipped with a compatible IEEE-488 interface card to program all controllable elements connected to the Four Bit Parallel Bus in the UTI-1. The computer can either "write" to devices connected to the bus or "read" from them.

The address of the IEEE-488 Bus can be set by an eight position DIP switch mounted on the component side of the circuit board. The allowable addresses are any number between zero and thirty-one.



X = Switch position does not matter

Figure 3.1.2 IEEE-488 Bus Address Switch (SW 1)

3.1.2 Control of UTI-1 Modules

Data transfer between the controller and up to fifteen UTI-1 modules is enabled by the Four Bit Parallel Bus via the UTI-1 motherboard. The fifteen card select lines (CS1 through CS15), each routed to a separate card slot (card position), enable the selection of a single UTI-1 module for each transaction. Once the modules have been individually programmed, event sequences can be controlled using two available trigger lines (TRIG-1 and TRIG-2). For more information on programming these modules, see the programming sections 3.2.4 and 3.2.5.

3.1.3 Interchangeable Test Adapter (ITA) Control

The personality circuit on the Interchangeable Test Adapter (ITA) is controlled by latched lines on connector BU1 of this module or additional latched lines on the Standard Latch Module (BN 9537/00.24).

On the IEEE-488 Interface module, the Four Bit Parallel Bus controls the status of eight separate relay driver lines, and senses the condition of eight individual TTL level inputs connected to the ITA. In addition, the Four Bit Parallel Bus can read the specific ITA ID number. For more information on the control of these lines, see the programming description section.

When additional control of the personality circuit is needed, the Standard Latch Module can be used. This module has 38 separate talk lines, and 8 separate listen or sense lines. When using the talk lines to drive relays, appropriate relay drivers must be provided on the personality circuit of the ITA. See the description of the Standard Latch Module for more information.

3.1.4 ITA Identification Number

Each ITA can have a unique identification number which enables the operating program to differentiate between different Interchangeable Test Adapters (ITA). This feature will ensure that the proper ITA is connected. The eight bit ID number is read via the Four Bit Parallel Bus four bits at a time by interrogating positions D and E of the IEEE-488 Interface Module. Position E contains the four least significant bits. See the programming section for more information on using this feature.

3.1.5 Mechanical Start Switch

A plug-in jack (Bu 4) is provided on the rear panel of the IEEE-488 Interface Module. Two switches can be connected to this jack. The status of the two mechanical switches is determined by interrogating character F and determining the status of the two least significant bits (20 and 21) of the received data. See the programming section for more information on using this feature.

3.1.6 External Instrument Control

External instruments with BCD remote control interfaces can be connected to the External Control Expansions Connector (Bu 2) via buffer store (parallel latch) circuits. Buffer stores are parallel latches capable of holding programmed data in BCD format. The External Control Expansion Connector is an expansion of the Four Bit Parallel Bus.

Up to eleven buffer stores can be connected to connector Bu2. Each buffer store must have a separate auxiliary equipment address. The auxiliary equipment address is determined by the four address lines (pins 5, 17, 6, and 18) connected to Bu2. The address range for external buffer stores must conform to Table 3.1.2, which allows a maximum of eleven (0 through 15 except 1, 2, 3, 9, and 14).

Table 3.1.2 Auxiliary Equipment ADDRESS Assignments

Addr Bits 2^3	2^2	2^1	2^0	Decimal Number	Assigned Equipment
0	0	0	0	0	Buffer Store
0	0	0	1	1	UTI-1
0	0	1	0	2	TRIG-1 *
0	0	1	1	3	TRIG-2 *
0	1	0	0	4 through 8	Buffer Store
1	0	0	1	9	RESET **
1	1	1	0	14	Reserved for firmware use
1	1	1	1	15	Buffer Store

* $\overline{\text{TRIG-1}}$ and $\overline{\text{TRIG-2}}$ lines are used to initiate events in modules connected to the UTI-1 Motherboard. Refer to sections 3.2.4 and 3.3.2 for further information on these two lines.

** The $\overline{\text{RESET}}$ line can be used to reset the modules connected to the UTI-1 Motherboard. Refer to sections 3.2.4 and 3.3.2 for further information on this line.

3.2. Programming

The programming of the IEEE-488 Interface Module has two basic purposes. The primary purpose is to control UTI-1 modules and external instruments via the Four Bit Parallel Bus. The second purpose is to control some internal functions of this module. Section 3.2.3 has the details on programming the internal functions and section 3.2.4 contains the details on programming the external devices.

3.2.1 Writing to Devices on the Four Bit Parallel Bus

Writing to devices using the IEEE-488 Interface Module is done by using WRITE control blocks. The Four Bit Parallel Bus WRITE control blocks have the following format:

OUTPUT 701;"W X S_1 S_2 a b c d e f g h i j k l m n o p"

Where:

OUTPUT: Output data statement required by the HP 9000 200/300 series computer.

7: Computer related I/O plug-in (IEEE-488 Interface) address.

01: IEEE-488 Interface Module address.

W: Word identifier "W" identifies the string as a write command.

X: Auxiliary equipment address: An address that is used only by the computer interface module in slot 0 to differentiate between the internal Four Bit Parallel Bus and the Buffer Stores (parallel latches) connected to Control Expansions Connector Bu 2. The internal parallel bus includes the internal functions of this module and the motherboard connections. The auxiliary equipment address of the internal bus is "1".

S_1: Starting Position Selector. This specifies the first address in the data transfer. It must be in the range A to P.

S_2: Ending Position Selector. This specifies the last address in the data transfer. It must be in the range A to P and equal to or greater than S_1.

a-p: The actual data to be transferred over the four talk lines. Since there are 16 possible values, each position is coded as one of the 16 consecutive ASCII characters starting with "0" (0123456789:;<=>?). The first character corresponds to the data sent to the address specified in S_1. Each additional character determines the data sent to each successive address until S_2 is reached. The number of data characters must match the range of data positions specified by S_1 and S_2.

3.2.2 Reading from devices on the Four Bit Parallel Bus

Reading from devices on the Four Bit Parallel Bus is done using INTERROGATE control blocks. INTERROGATE control blocks in the Four Bit Parallel Bus are of the following format:

OUTPUT 701; "I X S_1 S_2"

Where:

OUTPUT: Output data statement required by the HP 9000 200/300 series computer.

7: Computer related I/O plug-in (IEEE-488 Interface) address.

01: IEEE-488 Interface Module address.

I: Identifies the string as a read command.

X: Auxiliary equipment address: An address that is used only by the computer interface module in slot 0 to differentiate between internal 4 Bit Parallel Bus and the Buffer Stores (parallel latches connected to Control Expansion Connector BU2. The internal parallel bus includes the internal functions of this module and the motherboard connections. The auxiliary equipment address of the internal bus is "1".

S_1: Starting Position Selector. This specifies the first address in the data transfer. It must be in the range A to P.

S_2: Ending Position Selector. This specifies the last address in the data transfer. It must be in the range A to P and equal or greater than S_1.

The "I" command specifies the range of data positions to sequentially output to the system controller by a read operation.

3.2.3 Programming Internal Functions

All internal functions of the IEEE-488 Interface Module are written to and read from by using the card select "0" and auxiliary address "1".

Table 3.2.2 Controlling internal functions

Function (Talk)	A	B	C	D	E	F	G	H	Notes
Card Select	0								
Clear Start Switches 1 and 2		0							1
Enable Start Switch 1		1							
Enable Start Switch 2		2							
Clear Relay Drive Lines 1 and 2			0						1, 2
Activate Relay Drive Line 1			1						
Activate Relay Drive Line 2			2						
Clear Relay Drive Lines 3 and 4				0					1, 2
Activate Relay Drive Line 3				1					
Activate Relay Drive Line 4				2					
Clear Relay Drive Lines 5 and 6					0				1, 2
Activate Relay Drive Line 5					1				
Activate Relay Drive Line 6					2				
Clear Relay Drive Lines 7 and 8						0			1, 2
Activate Relay Drive Line 7						1			
Activate Relay Drive Line 8						2			

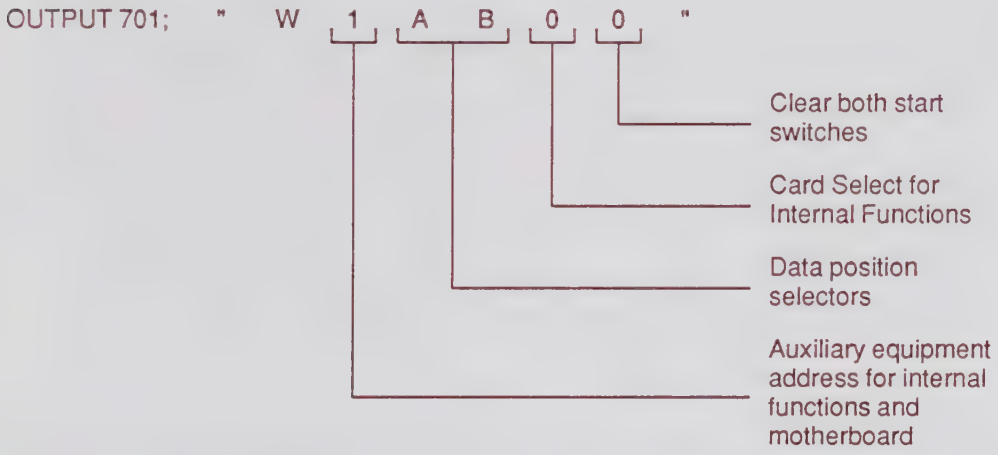
Notes:

1. If more than one function is desired, add corresponding data.
2. Relay drive lines go low when activated.

3.2.3.1 Programming Start Switches

Programming the start switches on the rear panel is done by programming position B of the WRITE control block. The switches must first be cleared before they are activated.

1. **Clear both switches.**

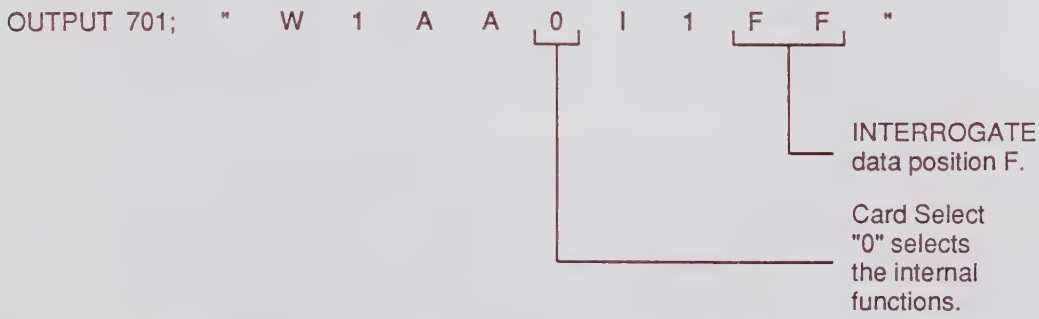


2. **Set start switches.** By programming a "1" or a "2" in data position B, either start switch 1 or start switch 2 can be activated. By programming a "3" in this position, both start switches are activated. In the following example both switches are activated.

OUTPUT 701; "W1AB03"

Note: The "0" in data position A does not need to be written to if the last output statement contained the card select "0". In that case the statement "W1BB3" will suffice.

3. **Read start switches.** The start switches are read by data position F. With no switches pressed, this position will read 12 (ASCII character "<"). When S_1 is pressed, this position will read 13 (ASCII character "="). When S_2 is pressed, this position will read 14 (ASCII character ">").



If the last Card Select address specified by the operating program was 0, then the output statement in sample 2 can be executed as follows:

OUTPUT 709;"I1FF"

This is possible because the card select information is latched and will not change unless a WRITE control block that specifies a different value on the "A" position is executed.

Note: Spaces between each character in the above example are used for illustrative purposes only.

The information can now be read by the controller using an ENTER command and storing the result into a string variable.

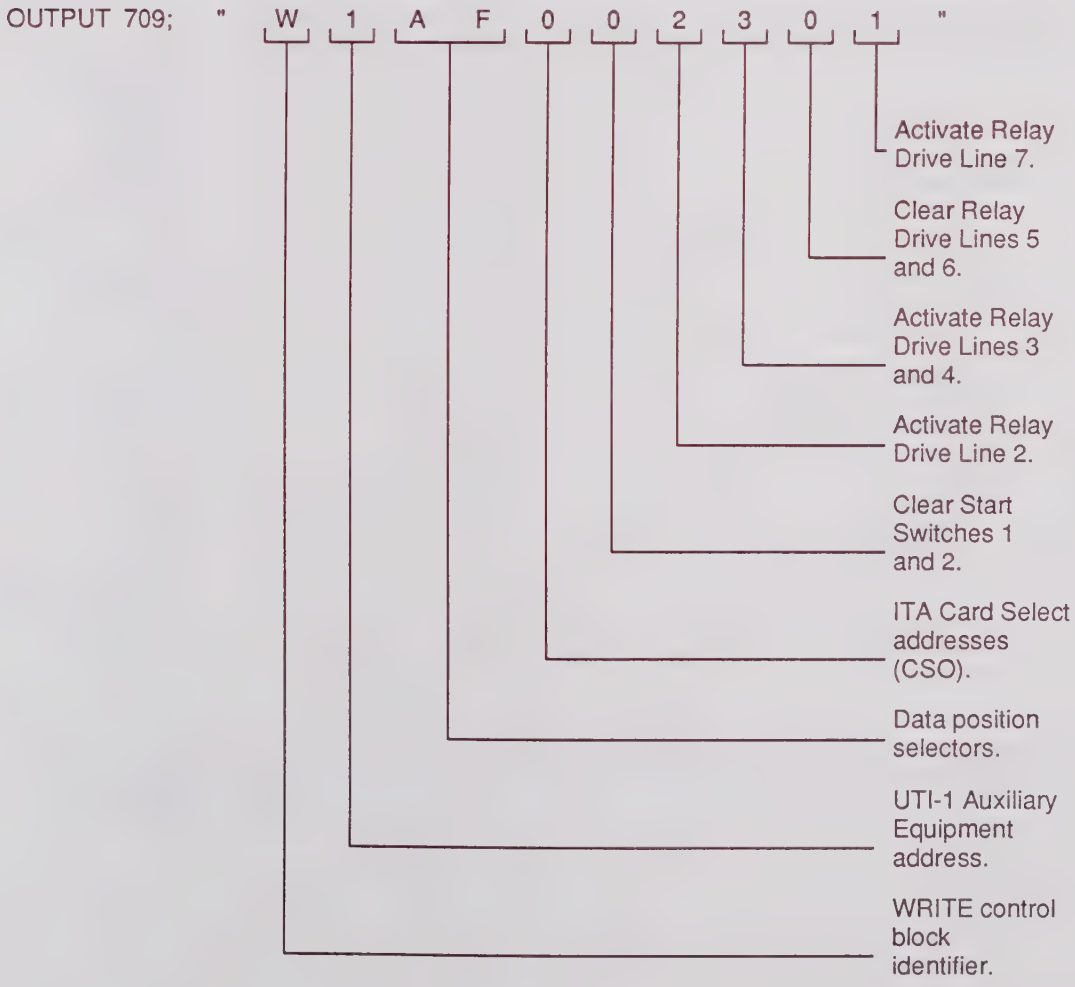
ENTER 701;Result$

3.2.3.2 Programming the Relay Drivers

The relay drivers are programmed in data positions C, D, E, and F. The auxiliary equipment address is "1" and the card select address information in character "A" of a WRITE control block is "0". See Table 3.2.

The relay drivers are controlled in pairs.
Data position C controls driver lines 1 and 2;
data position D controls driver lines 3 and 4;
data position E controls driver lines 5 and 6;
and data position F controls driver lines 7 and 8. When the driver lines are cleared, these lines are set high. When the driver lines are activated these lines are pulled low.

Sample:



If the last Card Select address specified by the operating program was 0, then the output statement in sample 2 can be executed as follows:

OUTPUT 709;"W1CF2301"

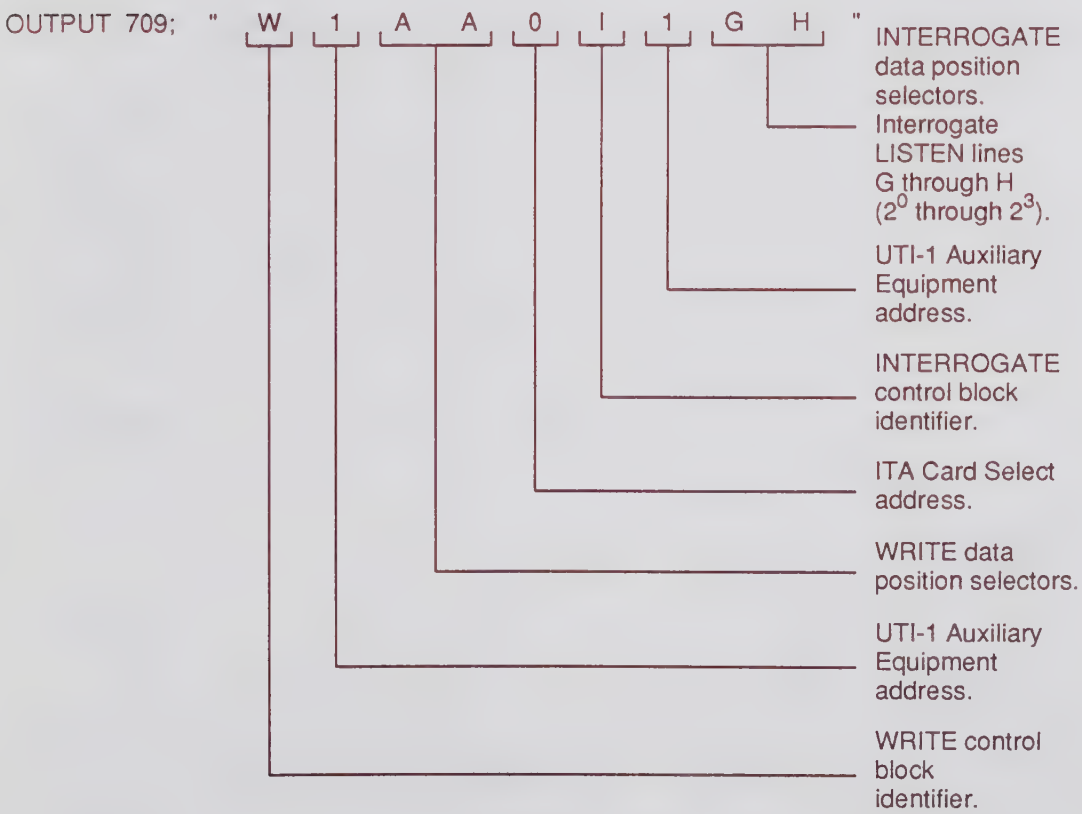
This is possible because the card select information is latched and will not change unless a WRITE control block that specifies a different value on the "A" position is executed.

Note: Spaces between each character in the above examples are used for illustrative purposes only.

3.2.3.3 Reading the Status of the Listen Lines from the ITA

Reading the status of the listen lines from ITA is done by interrogating data positions G & H. The auxiliary equipment address is "1" and the card select address information in character "A" of a WRITE control block is "0". See Table 3.2.

Sample 1:



Sample 2:

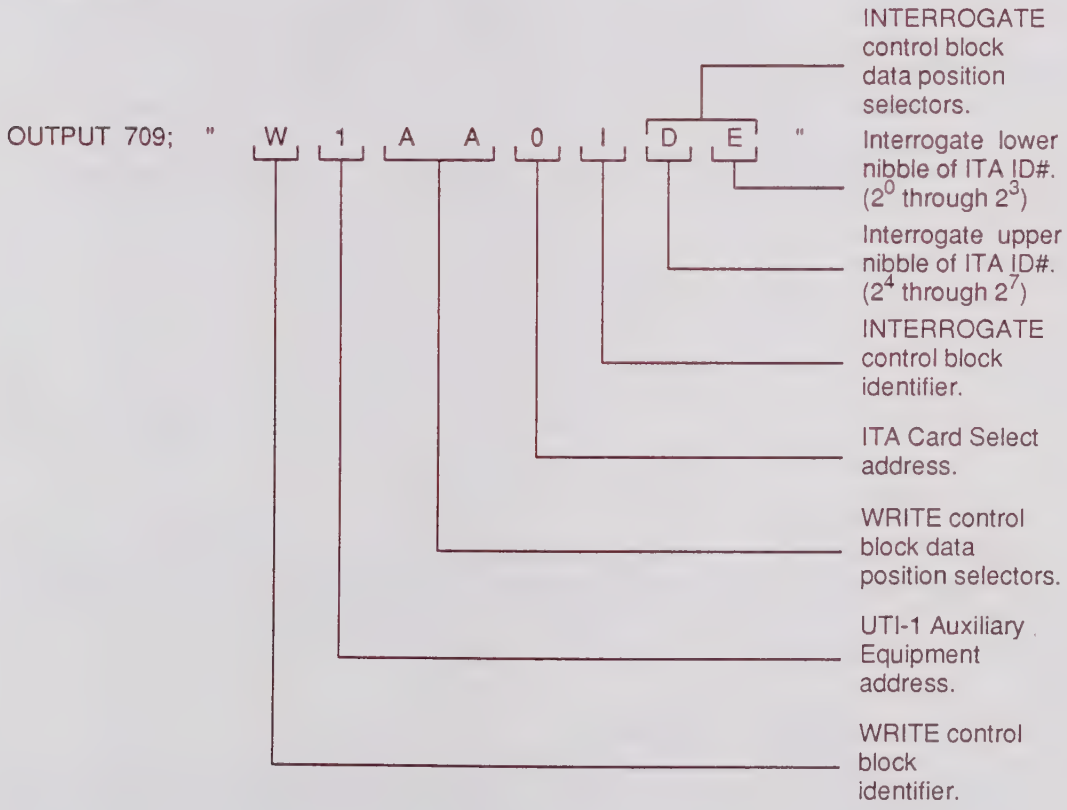
ENTER 709; M $

Computer related. Denotes the string variable which will accept the data from positions G and H as programmed above in Sample 1.

3.2.3.4 Reading the ITA Identification Number

Reading the ITA identification number is done by interrogating data positions D & E. The auxiliary equipment address is "1" and the card select address information in character "A" of a WRITE control block is "0". See Table 3.2.

Sample 1:



This word sets up the IEEE-488 Interface module as a talker and sets up the Four Bit Parallel Bus to transfer data from the ITA to the controller. The actual computer "READ" is shown in sample 2 below:

Sample 2:

```
ENTER 709; M    $
```

Computer related. Denotes the string variable which will accept the data from positions D and E as programmed above in Sample 1.

Since binary number 2^0, 2^1, 2^2 and 2^3 are read back in data position E and binary numbers 2^4, 2^5, 2^6 and 2^7 are read back in data position D, the information in M$ must be converted to a decimal ID number. Since the ASCII characters in each position represent 0 through 15, the result can be treated as a HEX number.

Note: The actual characters read back in each data position will be the ASCII characters 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, :. ;, <, =, > and ? which correspond to the HEX characters 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, and F respectively.

Position D data		Position E data		Actual ID Number	
Binary Equivalent	Decimal Equivalent	Binary Equivalent	Decimal Equivalent	Binary Equivalent	Decimal Equivalent
2^0	1				1
2^1	2				2
2^2	4				4
2^3	8				8
		2^0	1		16
		2^1	2		32
		2^2	4		64
		2^3	8		128

For example:

An ITA number of 38 is required. Data position D will read back a 2 corresponding to the corresponding to an ID number of 32, and data position E will read back a 6 corresponding to an ID number of 6. The result from the variable M$ will be "26". The decimal equivalent of the HEX number 26 is 38.

3.2.4 Controlling the UTI-1 Modules

The UTI-1 modules are controlled by using the auxiliary equipment address "1" and the card select number representing the desired module. The first character in data position "A" is decoded to a card select. This data is equivalent to the slot number containing the module. Therefore, the hardware on the UTI-1 modules must be designed to ignore the "A" position selection.

Additional functions of the IEEE-488 Interface Module provide sequential event control and global hardware reset to the UTI-1 modules. Two trigger lines ($\overline{\text{TRIG-1}}$ and $\overline{\text{TRIG-2}}$) are controlled independently to initiate separate events. One reset ($\overline{\text{RESET}}$) line connected to the UTI-1 Motherboard can be used to clear the status of the UTI-1 modules which make use of this line.

Sample 1:

OUTPUT 7 0 9 ; " W 1 A C 5 9 ? "

W: selects data transfer direction as to the UTI-1 module.

1: Auxiliary Equipment Address for the UTI-1.

A: The first element addressed is A

C: The last element addressed is C

5: element A receives the binary equivalent of ASCII 5 or 0101, corresponding to the state of the four Talk lines. The "5" in this position directs the following data to the module in slot 5. This card select information is latched in the computer interface and will not change unless a program word is sent that writes a different value in the "A" position. For example if the next programing word sent is "W1BC12", the information in positions "B" and "C" will be again sent to the module in slot 5.

9: element B receives the binary equivalent of ASCII 9 or 1001.

?: element C receives the binary equivalent of ASCII ? or 1111.

The trigger and reset functions of the IEEE-488 Interface Module are programmed using WRITE control blocks with the respective Auxiliary Equipment Address. Refer to table 3.2.4.

Table 3.2.4 Auxiliary Equipment ADDRESS Assignments for the UTI-1 Universal Test Interface.

Addr Bits 2^3	2^2	2^1	2^0	Decimal Number	Assigned Function
0	0	0	1	1	UTI-1
0	0	1	0	2	$\overline{\text{TRIG-1}}$
0	0	1	1	3	$\overline{\text{TRIG-2}}$
1	0	0	1	9	$\overline{\text{RESET}}$
1	1	1	0	14	Reserved for firmware use

Sample 2:

OUTPUT 7 0 9 ; " W 2 "

W: selects data transfer direction as to the UTI-1 module.

2: Auxiliary Equipment Address for $\overline{\text{TRIG-1}}$ line.

This output statement pulses a low transition (about 40 Sec) on the $\overline{\text{TRIG-1}}$ line of the UTI-1 Motherboard.

Sample 3:

OUTPUT 7 0 9 ; " W 9 "

W: selects data transfer direction as to the UTI-1 module.

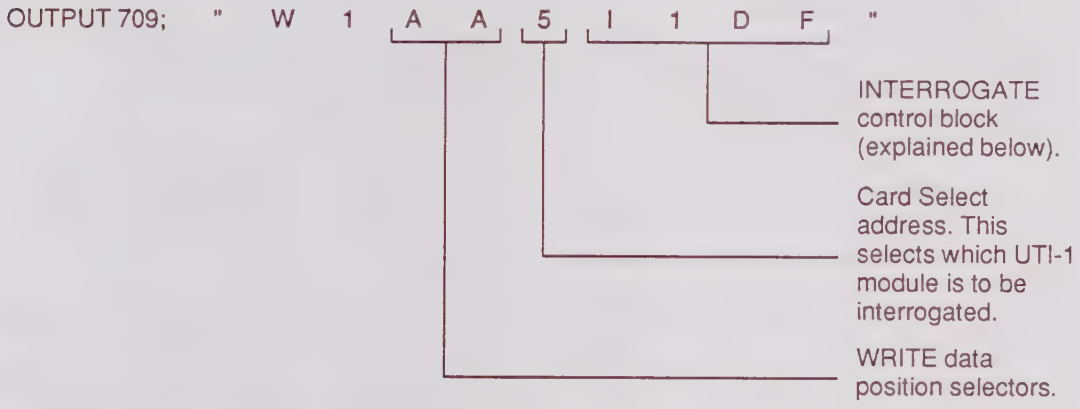
9: Auxiliary equipment address for $\overline{\text{RESET}}$ line.

This output statement pulses a low transition (about 40 µSec) on the $\overline{\text{RESET}}$ line of the UTI-1 Motherboard.

3.2.5 Reading from UTI-1 Modules

The UTI-1 modules are interrogated by using the auxiliary equipment address "1" and the card select number representing the desired module. The first character in data position "A" is decoded to a card select. This data is equivalent to the slot number containing the module. The hardware on the UTI-1 modules must be designed to ignore the "A" position selection.

Sample 1:



This word sets up the IEEE-488 Interface Module to become a talker and sets up the Four Bit Parallel Bus to transfer data from the addressed UTI-1 module to the controller. The actual computer related "READ" statement is shown in sample 2 below.

"I1DF" explained.

I: Selects data transfer as to the system controller.

1: Auxiliary equipment address for the UTI-1.

D: The first element to be transferred is D.

F: The last element to be transferred is F.

Note: The INTERROGATE control blocks used for reading from the UTI-1 Modules cannot address the "A" position. Therefore, it is necessary to precede an interrogate command with a write command specifying the module to be addressed. In the above example, if the module in slot 5 was the last module addressed, that module will still be selected. In that case, it would suffice to send only the "I" (interrogate command).

Sample 2:

ENTER 7 0 9 ; M$

M$ is the string variable which will accept the data from positions D, E, and F as programmed above in sample 1.

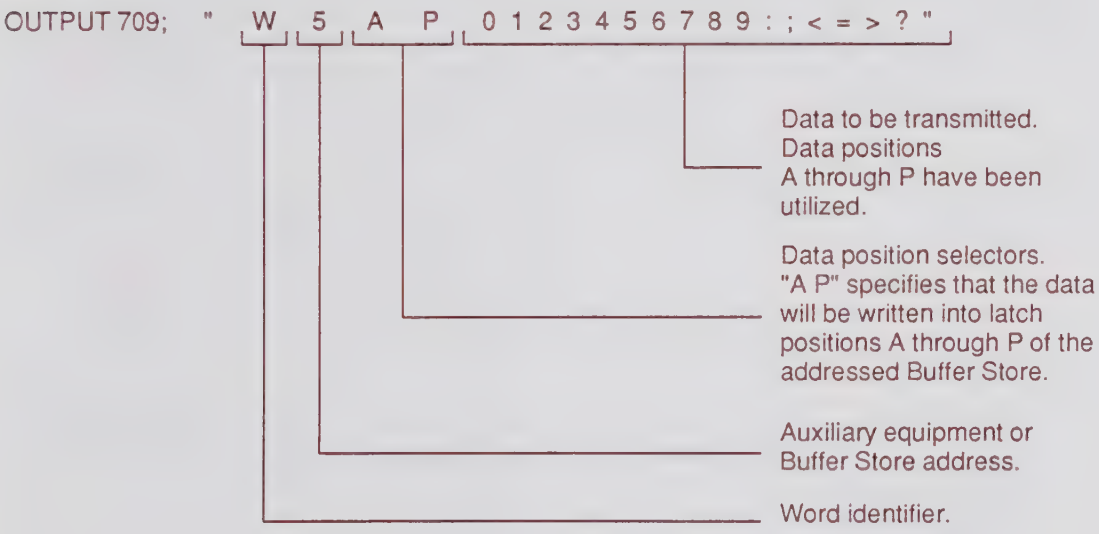
In the preceding examples the data contained in positions D, E, and F are transferred from the module in slot 5 to the controller via the 4 Bit Parallel Bus.

3.2.6 Writing to Buffer Stores

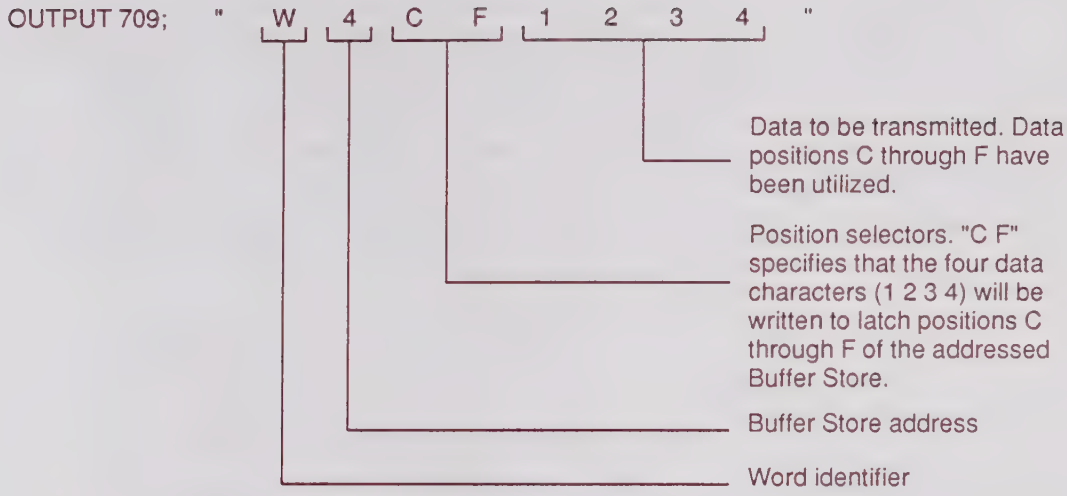
Writing to buffer stores (external parallel latches) is accomplished through the external control expansion connector. Different buffer stores can be selected by using different Auxiliary equipment addresses. This address is set on each buffer store and must conform to Table 3.1.2.

In the following example, a Buffer store designed for data positions A through P has been written to.

Sample 1:



Sample 2:



Note: Spaces between each character in the examples above are used for illustrative purposes only.

Sample 3:

```
OUTPUT 709;"W4AC123W5CD12W3AH12345678"
```

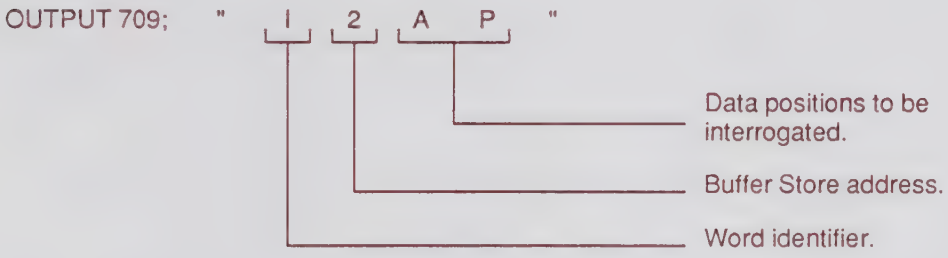
In the above example, the total string contains three WRITE control blocks. The IEEE-488 Interface module is capable of receiving a string of multiple control blocks.

3.2.7 Reading from Buffer Stores

Interrogating buffer stores (external parallel latches) is accomplished through the external control expansion connector. Different buffer stores can be selected by using different Auxiliary equipment addresses. This address is set on each buffer store and must conform to Table 3.1.2.

In the following example, a Buffer store designed for data positions A through P is interrogated.

Sample 1:



This INTERROGATE control word sets up the IEEE-488 Interface module to become a talker and the Four Bit Parallel Bus interface to transfer data from the Buffer Store to the controller. The actual computer related "READ" statement is shown in sample 2 below.

Sample 2:

ENTER 7 0 9 ; M $

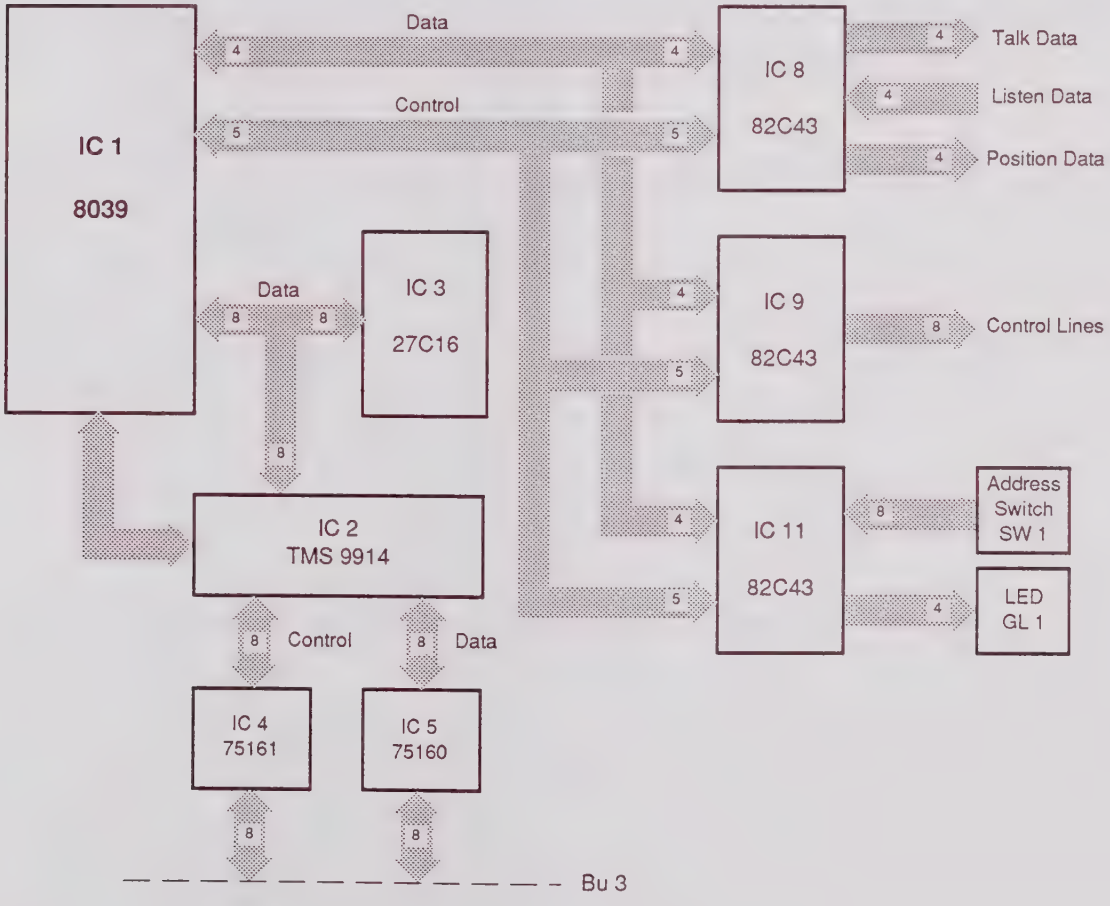
M$ is the computer related string variable which will accept the data from positions A through P as programmed in sample 1 above.

3.3. Circuit Description

3.3.1 Microprocessor Interface Circuitry

The circuitry which interfaces with the microprocessor consists of IC1 through IC11. The General Purpose Interface Bus (GPIB), which contains the IEEE-488 signals, is connected to Bu 3. IC4 and IC5 assure the proper signal level of incoming and outgoing signals. IC2 implements the link between the GPIB bus and the microprocessor IC1. The EPROM IC3 contains IC1's firmware instructions. The generation of all the signals required in the Four Bit Parallel Bus is made possible by the bus expanders IC8 and IC9.

Figure 3.3.1 Interface Circuit Block Diagram



When an OUTPUT statement is sent by the controller, IC1 interprets incoming data from the IEEE-488 Bus Controller. Each data character is read from the IEEE-488 Bus as an 8-bit ASCII character. IC1 strips off the four left most bits of all incoming characters (Talk Data) and writes binary data to IC8 and IC9 according to firmware instructions in IC3. The TALK data is first written to IC8 immediately followed by POSITION data. Control data is written to IC9 to control the sequence and direction of the data transfer.

When an ENTER statement is sent by the controller, IC1 retrieves four binary bits per character from IC8 (Listen Data). IC1 then attaches binary numbers 0011 to the four left most bits of the retrieved character before sending it to the bus controller. The result of this operation is that only the following ASCII characters are used for data transfer in the Four Bit Parallel Bus:

0,1,2,3,4,5,6,7,8,9,:,;,<,=,>,?

The ADDRESS SWITCHES and MONITOR LEDs functions performed via IC11 are described in sections 3.3.9 and 3.3.10 respectively.

3.3.2 Four Bit Parallel Bus Architecture on the UTI-1 Motherboard

Modules connected to the UTI-1 Universal Test Interface are controlled by the Four bit Parallel Bus via Motherboard connector ST2. Figure 3.3.2 is a simplified block diagram of this circuitry.

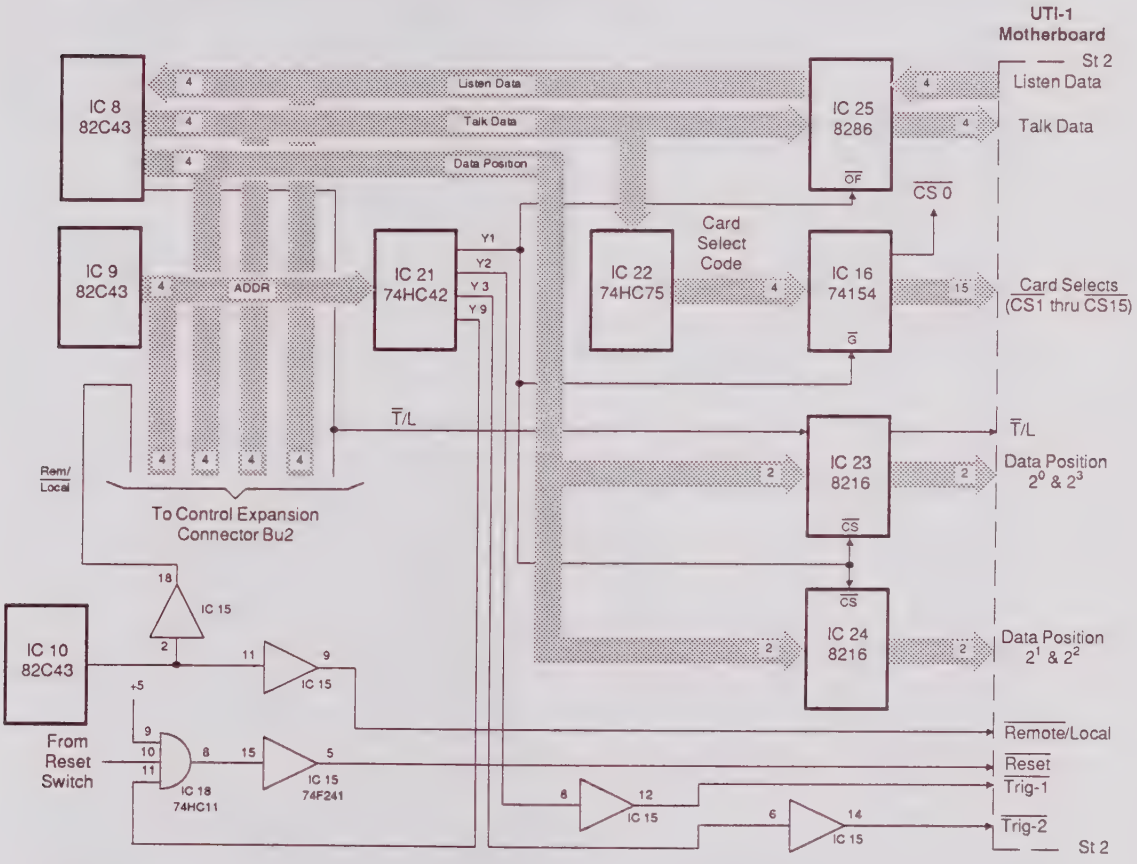


Figure 3.3.2 Motherboard Four Bit Parallel Bus Block Diagram

The four LISTEN DATA lines (LISTEN 2^0, LISTEN 2^1, LISTEN 2^2, LISTEN 2^3) are used to read data from the controlled elements. These lines originate at Motherboard connector ST2 (pins 44B, 43B, 42B, and 41B). Transceiver IC25 buffers these signals for bus expander IC8. During INTERROGATE control blocks, IC1 reads the LISTEN DATA lines from IC8 and appends the four leftmost bits to the data retrieved from each character position. The range of the binary data is 0 through 15. Data above 9 will be assembled in the IEEE-488 Interface Module as ASCII characters :,;,<,=,>, and ?. Once each character is assembled, IC1 sends the ASCII character to IC2. IC2 outputs each character to the computer via IC4 and IC5 by following the IEEE-488 bus communication protocol. The logic of the LISTEN DATA lines is positive true.

The four TALK DATA lines (TALK 2^0, TALK 2^1, TALK 2^2, TALK 2^3) originate in bus expander IC8 and are coupled to Motherboard connector ST2 (pins 44A, 43A, 42A, and 41A) via transceiver IC25. These lines provide the command data to the controlled element. During the execution of WRITE control blocks, microprocessor IC1 strips off the four leftmost bits of the ASCII characters sent by the computer and outputs the four right-most bits to the TALK DATA lines. The range of binary data is the ASCII characters 0 through 9, :, ;, <, =, >, and ?. The logic of these lines is positive true.

CARD SELECT lines 1 through 15 are used to select individual UTI-1 modules. CARD SELECT line 0 is used internally by the IEEE-4888 Interface Module to communicate with the ITA, as well as to control and query the status of Mechanical Start Switches 1 and 2. For each control block, a single CARD SELECT code is latched into bistable latch IC22. Demultiplexer IC16 decodes the output code from IC22 into a single CARD SELECT line of Motherboard connector ST2. During WRITE and INTERROGATE control blocks IC1 strobes IC16 to send one low pulse for each data character within the block. Data in the "A" position (card select data) determines the card select code to be latched into IC22. Therefore, all modules connected to the Four Bit Parallel Bus through the UTI-1 Motherboard should be designed to ignore the "A" data position in the WRITE mode (see section 3.3.2.1 for further information).

The four DATA POSITION lines (POS 2^0, POS 2^1, POS 2^2, POS 2^3) are used to indicate the position of each character in either WRITE or INTERROGATE control blocks. These lines originate in bus expander IC8 and are coupled to Motherboard connector ST2 (pins 50A, 49A, 48A, and 47A) via bus drivers IC23 and IC24. During WRITE and INTERROGATE cycles, IC1 transfers the data position code for each character into bus expander IC8. The card select lines and these position lines provide the means of addressing specific hardware elements. While the card select lines select a particular module, the data position lines select one of sixteen possible latches (each latch is 4 bit binary) within the selected module. Table 3.3.2 shows the binary value for each character position. The logic of these lines is positive true.

DATA POSITION code 2^3	2^2	2^1	2^0	TALK DATA character
0	0	0	0	A
0	0	0	1	B
0	0	1	0	C
0	0	1	1	D
0	1	0	0	E
0	1	0	1	F
0	1	1	0	G
0	1	1	1	H
1	0	0	0	I
1	0	0	1	J
1	0	1	0	K
1	0	1	1	L
1	1	0	0	M
1	1	0	1	N
1	1	1	0	O
1	1	1	1	P

Table 3.3.2 Binary Representation of each Character Position

The $\overline{T}$/L line is used to indicate the direction of data in the Four Bit Parallel Bus. This line originates in pin 17 of bus expander IC8 and is coupled to Motherboard connector ST2 (pin45A) via bus driver IC23. During a WRITE control block (talk mode), microprocessor IC1 maintains this line low. During INTERROGATE control blocks (listen mode), IC1 maintains this line high.

The $\overline{\text{REMOTE}}$/LOCAL line is set low (remote) or high (local) by the controller via the controller interface module. This line can be used to arm UTI-1 Modules and, if necessary, to set the controlled instrument in remote or local mode.

The $\overline{\text{RESET}}$ line can be controlled by Interface Reset Switch SW2 or by software control. This line is decoded by IC18 and coupled to Motherboard connector ST2 (pin 49B) via bus driver IC15. Pressing SW2 clears IC2 and causes a low to appear at pin 8 of IC18 and pin 49B of Motherboard connector ST2. Also, executing a WRITE control block with Auxiliary Equipment Address number nine (refer to table 3.1.2) decoded by IC21, will cause a low to be strobed at pin 8 of IC18.

Sample: The WRITE control block OUTPUT 709;"W9" will cause a low strobe of approximately 40 µSec to appear at pin 8 of IC18.

The low level on the $\overline{\text{RESET}}$ line purges the contents of all the latch circuitry of the modules connected to that line.

The two trigger lines ($\overline{\text{TRIG-1}}$ and $\overline{\text{TRIG-2}}$) are used to initiate events upon computer command. These lines are coupled to Motherboard connector ST2 (pins 48B and 47B) via bus driver IC15. The trigger lines are activated by programming WRITE control blocks with the Auxiliary Equipment Address that corresponds to the specific trigger line. The assigned Auxiliary Equipment Address for $\overline{\text{TRIG-1}}$ is "2" and for $\overline{\text{TRIG-2}}$ is "3" (refer to table 3.1.2).

Only the word identifier and the Auxiliary Equipment Address are required for the trigger WRITE control blocks that control each line.

Sample: The WRITE control block OUTPUT 709;"W2" will pulse the $\overline{\text{TRIG-1}}$ line low for approximately 40 Sec.

The WRITE control block OUTPUT 709;"W3" will pulse the $\overline{\text{TRIG-2}}$ line low for approximately 40 Sec.

Table 3.3.2 lists the UTI-1 Universal Test Interface Motherboard pin number assignment for the Four Bit Parallel Bus.

Table 3.3.2 Motherboard pin number assignment for the Four Bit Parallel Bus.

ST2 Pin	Signal Name	ST2 Pin	Signal Name
44A	TALK line 2^0	40A	Card Select line 1
43A	TALK line 2^1	39A	Card Select line 2
42A	TALK line 2^2	38A	Card Select line 3
41A	TALK line 2^3	37A	Card Select line 4
36A			Card Select line 5
44B	LISTEN line 2^0	35A	Card Select line 6
43B	LISTEN line 2^1	34A	Card Select line 7
42B	LISTEN line 2^2	40B	Card Select line 8
41B	LISTEN line 2^3	39B	Card Select line 9
38B			Card Select line 10
50A	POSITION line 2^0	37B	Card Select line 11
49A	POSITION line 2^1	36B	Card Select line 12
48A	POSITION line 2^2	35B	Card Select line 13
47A	POSITION line 2^3	34B	Card Select line 14
33B			Card Select line 15
49B	RESET line	45A	Talk/Listen line
48B	TRIGGER line 1		
47B	TRIGGER line 2	45B	$\overline{\text{Remote}}$/Local line

3.3.3 Control of UTI-1 Modules

Control of the UTI-1 Modules is accomplished via Mother board connector ST2. There are fifteen positions available in which the individual modules can be installed. Each position has its own individual card select line. The card select lines are numbered 1 through 15, where card select 1 corresponds to the module position closest to the IEEE-488 Interface Module and card select 15 corresponds to the module position farthest from the IEEE-488 Interface Module. Note that the IEEE-488 Interface Module must always be installed in the first slot on the right (slot 0) when viewing the rear panel of the UTI-1.

3.3.3.1 Writing to UTI-1 Modules

For the following discussion, refer to the IEEE-488 Interface Module schematic diagram. Microprocessor IC1 engages a talk mode sequence when it acknowledges a WRITE control block ("W _ _ _ _"). The steps taken by IC1 in the talk mode sequence are as follows:

1. Output binary 0011 (decimal 3) to port 7 of IC9. This directs transceivers IC23, IC24, and IC25 to place data in the ST2 direction. The binary code also sets up a high at pin 2 of IC19 to activate the 4-Bit Bus operation.
2. Output binary 1110 (decimal 14) to port 5 of IC9. This forces IC21 to drive all of its outputs (Y1 through Y9) high, which in turn disables IC16, IC23, IC24 and IC25.
3. Read 4-Bit Bus Auxiliary Equipment address byte and store it within IC1. For the UTI-1 Universal Test Interface this address must always be 1.
4. Read first and last data position bytes, take the difference of their lower 4-bits and store the result within IC1 as variable COUNT. Also, set POSITION data variable to the value of the first data position byte. If first data position byte is equal to ASCII Character A (card select address), set POSITION data variable to 0000. (See table 3.3.4)
5. Write a 0 to pin 17 (P63) of IC8. This activates the talk mode in the 4-Bit Bus circuitry.
6. Read talk data byte and output its lower 4-bits to port 4 of IC8.
7. Output the four lower bits of POSITION data variable to port 7 of IC8 (see Table 3.3.2).
8. Transfer the lower 4-bits of the 4-Bit Bus Auxiliary Equipment address byte read in steps 3 to port 5 of IC9; wait for 40 microseconds and then write 1110 (decimal 14) back to port 5 of IC9. The objective is to toggle pin 2 of IC21 so that it goes low for 40 microseconds.

   The card select address is latched into IC22 each time that the first data position code is 0000 (see step 7 above). Such code enables pin 12 of IC18 to go high when pin 9 of IC17 is driven low during the toggle of pin 2 of IC21. Consecutive toggles of pin 2 of IC21 do not affect the latched card select address in IC22 because consecutive data position codes in the POSITION data variable keep pin 12 of IC18 from going high again.

   Toggling pin 2 of IC21 enables transceivers IC23, IC24, and IC25 to place the data present at their inputs into connector ST2. However, data position and talk data must first be settled before the card select pulse is generated. Therefore, the transceivers are enabled first via pin 6 of IC19; then, R10 and C6 postpone the card select pulse by approximately 2 microseconds.
9. Decrease variable COUNT by one. If COUNT is not equal to zero, increment POSITION data variable and return to step number 6. If COUNT is equal to zero, the WRITE control block has ended.

   When a WRITE control block ends, IC1 looks for the next control block. The next control block could be a WRITE control block, an INTERROGATE control block (discussed below), or carriage return/line feed (CR/LF). When the next control block is CR/LF, the IEEE-488 Interface Module goes into idle state.

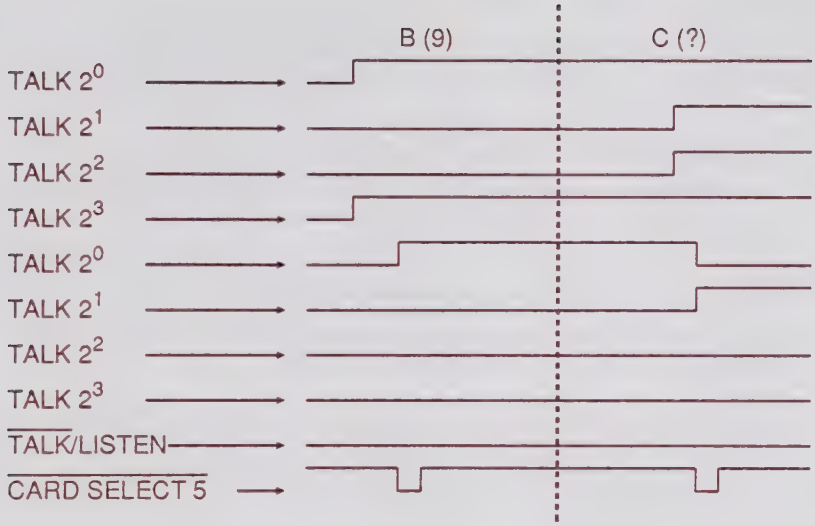


Figure 3.3.3.1 Transmission Sequence on the 4 Bit Parallel Bus in the Talk Mode

3.3.3.2 Interrogating UTI-1 Modules

For the following discussion, refer to the IEEE-488 Interface Module schematic diagram. The steps taken by microprocessor IC1 during an INTERROGATE control block ("I_ _ _) are the following:

1. Output binary 0001 (decimal 1) to port 7 of IC9. This sets transceiver IC25 to receive data from ST2.
2. Output binary 1110 (decimal 14) to port 5 of IC9. This disables IC16, IC23, IC24, and IC25.
3. Read Auxiliary Equipment address byte and store within IC1. For the UTI-1 Universal Test Interface this address must always be 1.
4. Read first and last position bytes, take the difference of their lower 4-bits and store the result as variable COUNT. Also, set POSITION data variable to the value of the first data position byte (see Table 3.3.2).
5. Write a binary 1 to pin 17 (P63) of IC8. This activates the listen mode in the 4-Bit Bus circuitry.
6. Write the lower 4-bits of POSITION data variable to port 7 of IC8.
7. Transfer the lower 4-bits of the Auxiliary Equipment address byte read in step 3 to port 5 of IC9. This causes a low level on pin 2 of IC22, which in turn enables IC16, IC23, IC24, and IC25. Note that the correct card select signal is generated due to the fact that the card select address was latched in IC22 on the previous WRITE control block. Therefore, the INTERROGATE control block must always be preceded by a WRITE control block to select the card which is to be interrogated.

8. Read listen data from port 5 of IC8 and transfer the ASCII equivalent byte to the controller via BU3. Since only four bits are read from port 5 of IC8, IC1 assembles the ASCII character by using the listen data for the lower 4-bits and attaching binary 0011 as the higher 4-bits. When byte transfer to the controller is complete, output binary 1110 (decimal 14) back to port 7 of IC9 to disable IC16, IC23, IC24, and IC25.
9. Decrease variable COUNT by one. If COUNT is not equal to zero, increment POSITION data variable and return to step 6. If count is equal to zero then go to idle state.

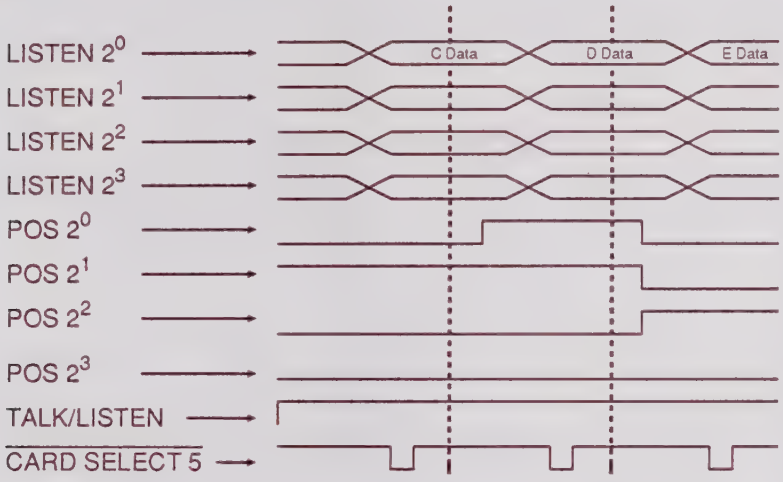


Figure 3.3.3.2 Transmission Sequence on the Four Bit Parallel Bus in the Listen (Interrogate) Mode

3.3.4 ITA Circuitry Connections

The IEEE-488 Interface Module provides direct control of circuit elements located on the personality module in the ITA. Figure 3.3.4a illustrates the circuitry dedicated for that purpose. Connector BU1 is the access port for personality modules on the ITA.

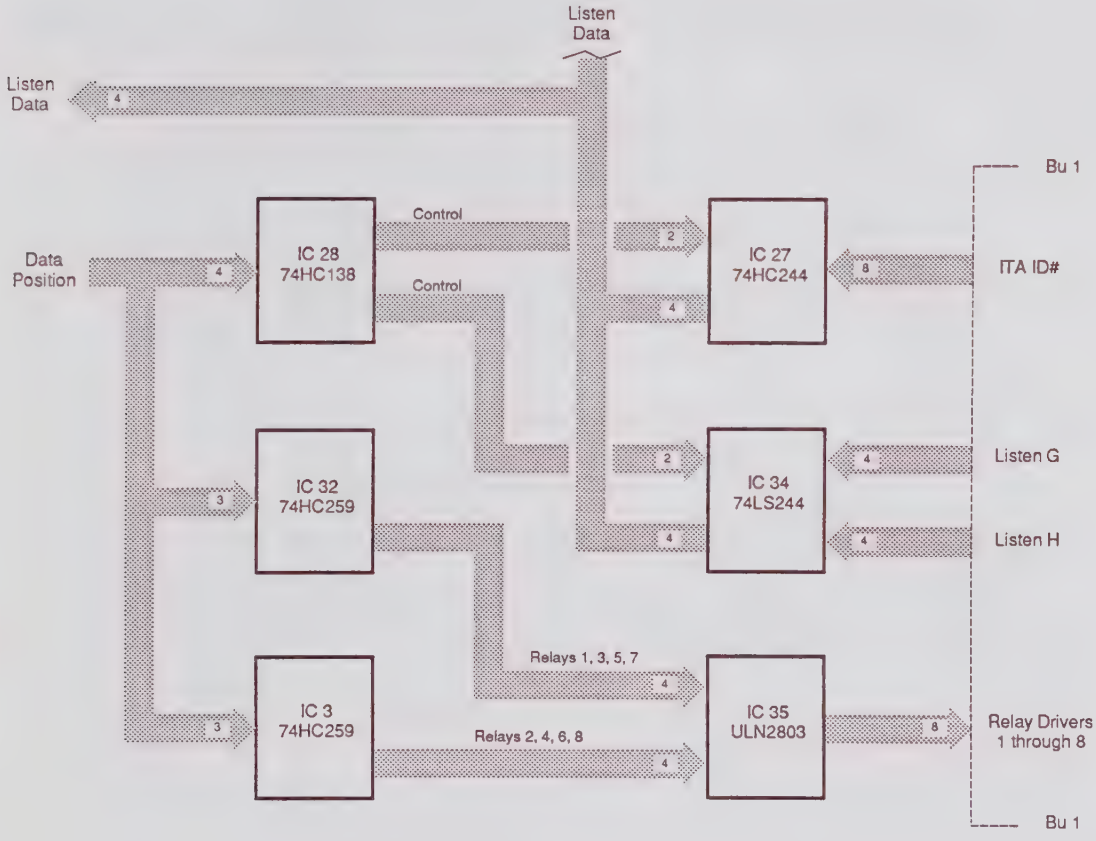


Figure 3.3.4a ITA Control Block Diagram

ITA Identification Number

The ITA Identification Number (ID #) is an 8-bit programmable code which is read by programming card select 0 and interrogating data characters "D" and "E" (see programming sheets, section 3.2.1). The DATA POSITION value for character "D" causes a low level at pin 12 of IC28, and enables IC27 to output the upper four bits of the ITA ID# (2^4 2^5 2^6 2^7) into the LISTEN DATA lines. The DATA POSITION value for character "e" causes a low level at pin 11 of IC28, and enables IC27 to output the lower four bits of the ITA ID# (2^0 2^1 2^2 2^3) into the LISTEN DATA lines. The 8-bit code is programmed by the user to identify individual personality boards. Figure 3.3.4b shows a block diagram of the ID# circuitry for the IEEE-488 Interface Module.

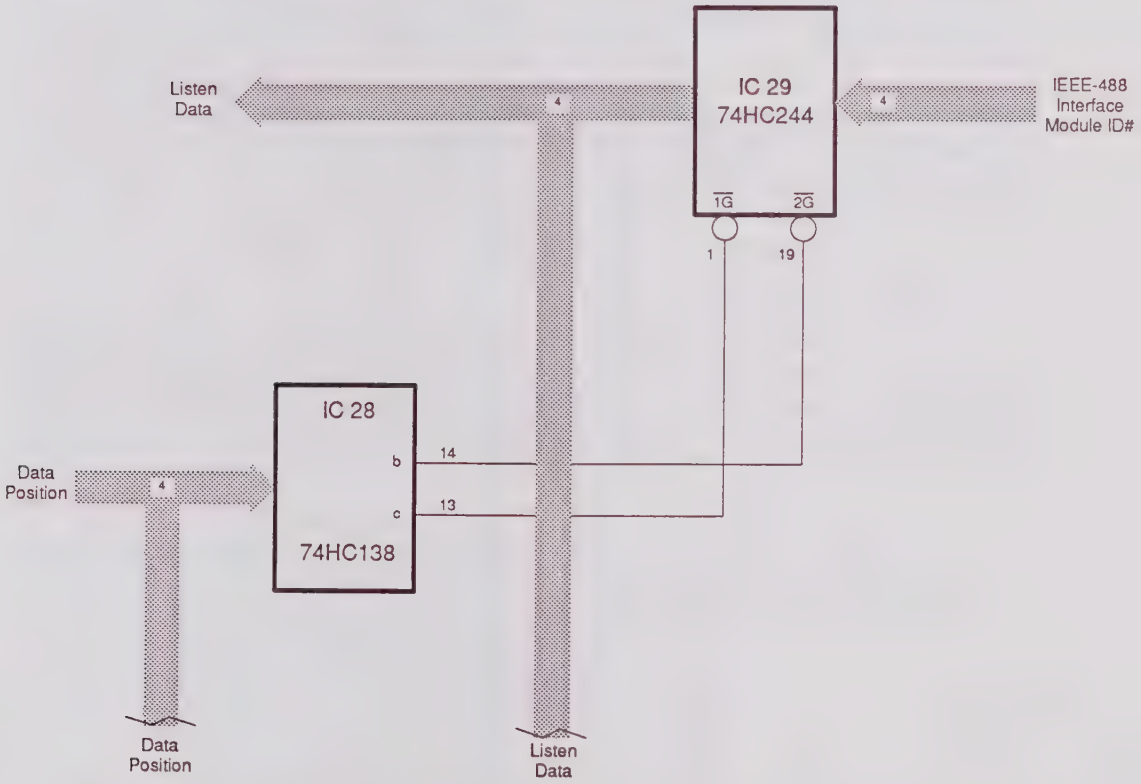


Figure 3.3.4b IEEE-488 Interface Module ID Number Circuit

ITA Listen Lines

Listen G and Listen H are eight lines used to determine circuitry status of the personality module. The status of eight separate circuit elements can be determined at any particular time by programming card select 0 and interrogating data characters "G" and "H" (see programming sheets, section 3.2.1). The DATA POSITION value for character "G" causes a low level at pin 9 of IC28, and enables IC34 to output the LISTEN G data (2^0 2^1 2^2 2^3) into the LISTEN DATA lines. The DATA POSITION value for character "H" causes a low level at pin 7 of IC28, and enables IC34 to output the LISTEN H data (2^0 2^1 2^2 2^3) into the LISTEN DATA lines.

ITA Relay Drivers

There are eight relay driver signals used to control the status of eight separate circuit elements on the UUT personality board at any given time The relays are controlled using card select 0 and programming data characters "C", "D", "E", and "F" (see section 3.2.1). DATA POSITION values for characters "C", "D", "E", and "F" enable either IC32 or IC33 to latch the oncoming TALK DATA. TALK 2^0 line is connected to IC32 and TALK 2^1 line is connected to IC33. IC32 controls the odd numbered relay drive lines, while IC33 controls the even numbered relay drive lines.

3.3.5 Mechanical Switch Activation

Connector BU4 is used to interface one or two mechanical switches, refer to figure 3.3.5. The mechanical switch activation is latched in IC31 and can be read by using card select 0 and interrogating data character "F" (see section 3.2.1). The DATA POSITION value for character "F" causes a low level at pin 10 of IC28, and enables the latched data in IC31 to be placed by IC30 onto the LISTEN DATA lines.

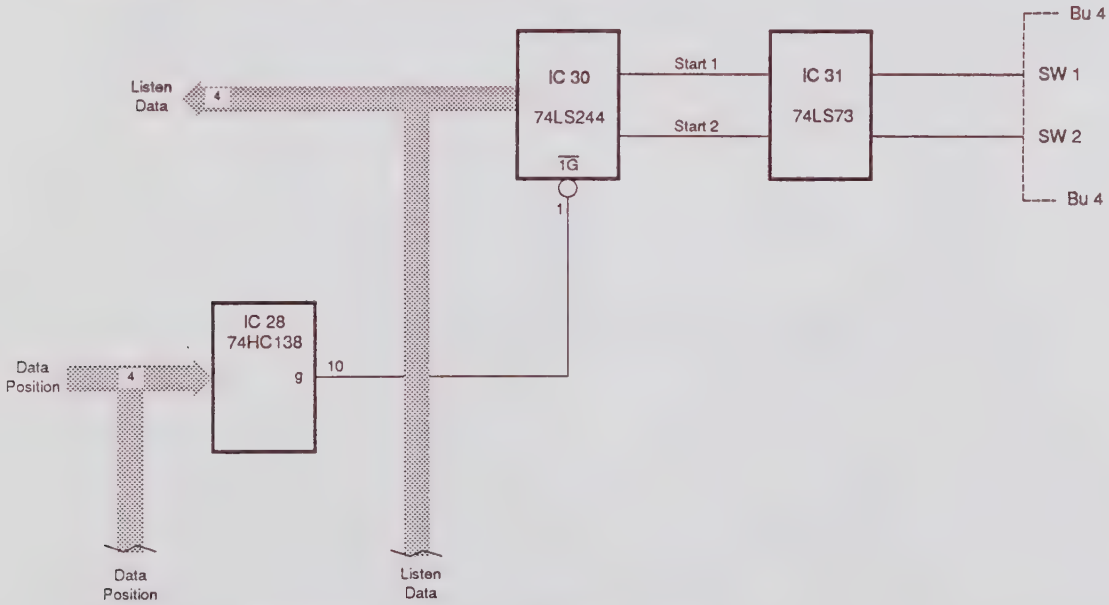


Figure 3.3.5 Mechanical Switch Circuit Block Diagram.

3.3.6 Four Bit Parallel Bus Architecture on the Control Expansion Connector

Control Expansion connector BU2 is used for controlling additional instruments via the Four Bit Parallel Bus. Buffer Stores are used as an interface between the Four Bit Parallel Bus and each additional instrument. Figure 3.3.6 shows a simplified diagram of this circuitry.

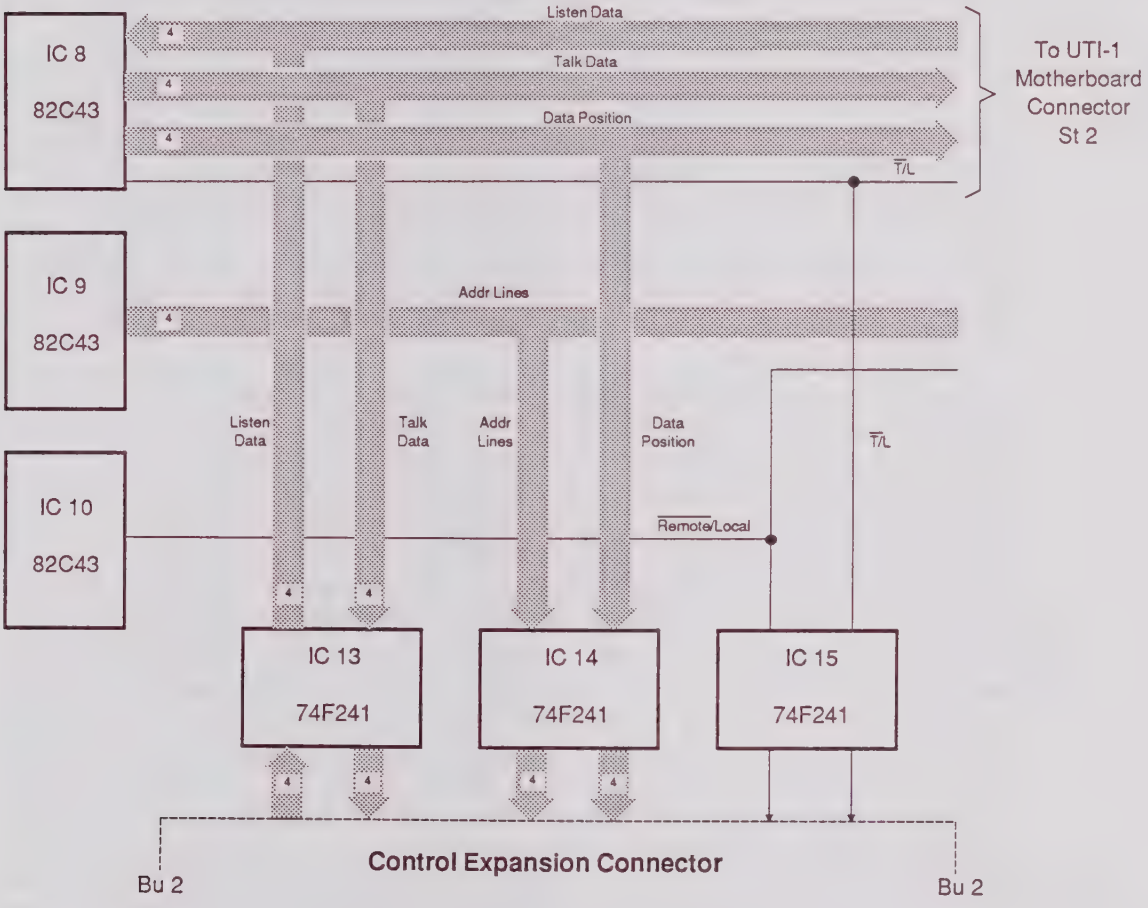


Figure 3.3.6 Control Expansion Connector Block Diagram

The four TALK DATA lines (TALK 2^0, TALK 2^1, TALK 2^2, TALK 2^3) originate in bus expander IC8 and are coupled to Control Expansion Connector BU2(pins 1, 13, 2, and 14) via bus driver IC13. These lines provide the command data to the controlled element. During the execution of WRITE control blocks, microprocessor IC1 strips off the four leftmost bits of the ASCII characters sent by the computer and outputs the four most right bits to the TALK DATA lines. The range of binary data is the ASCII characters 0 through 9, :, ;, <, =, >, and ?. The logic of these lines is positive true.

The four LISTEN DATA lines (LISTEN 2^0, LISTEN 2^1, LISTEN 2^2, LISTEN 2^3) are used to read data from the circuit controlled elements. These lines originate at Control Expansion Connector BU2 (pins 7, 19, 8, and 20) and IC13 buffers the signals for bus expander IC8. During INTERROGATE control blocks, IC1 reads the LISTEN DATA lines from IC8 and appends the four leftmost bits to the data retrieved from each character position. The range of the binary data is 0 through 15. Data above 9 will be assembled in the IEEE-488 Interface Module as ASCII characters :,;,<,=,>, and ?. Once each character is assembled, IC1 sends the ASCII character to IC2. IC2 outputs each character to the computer via IC4 and IC5 by following the IEEE-488 bus communication protocol. The logic of the LISTEN DATA lines is positive true.

The four Auxiliary Equipment Address lines (ADDR 2^0, ADDR 2^1, ADDR 2^2, and ADDR 2^3) provide the capability of addressing several Four Bit Parallel Bus instruments which use Buffer Store as the Four Bit Parallel Bus interface (Buffer Store addresses must conform to table 3.1.2). These lines originate in bus expander IC9 and are connected to Control Expansion Connector BU2 (pins 5, 17, 6, and 18) via bus driver IC14. During WRITE and INTERROGATE control blocks, microprocessor IC1 pulses the programmed Auxiliary Equipment Address code into IC8 once per each data character (see figures 3.3.2.1 and 3.3.2.2). Each time the programmed address code is pulsed, the data contents of one character is strobed into the addressed Buffer Store. The logic of these lines positive true.

The four DATA POSITION lines (POS 2^0, POS 2^1, POS 2^2, POS 2^3) are used to indicate the position of each character in either WRITE or INTERROGATE control blocks. These lines originate in bus expander IC8 and are coupled to Control Expansion Connector BU2 (pins 3, 15, 4, and 9) via bus driver IC14. During WRITE and INTERROGATE cycles IC1 transfers the data position code for each character into bus expander IC8. The Auxiliary Equipment Address (ADDR) lines and these position lines provide the means of addressing specific hardware elements. While the ADDR lines select a particular Buffer Store, the data position lines select one of sixteen possible latches (each latch is 4 bit binary) within the selected Buffer Store. Table 3.3.2 shows the binary value for each character position. The logic of these lines is positive true.

The $\overline{\text{REMOTE}}$/LOCAL line is set low (remote) or high (local) by the controller via the controller interface module. This line can be used to arm the Buffer Store and, if necessary, to set the controlled instrument in remote or local mode.

The $\overline{\text{T}}$/L line is used to indicate the direction of data on the Four Bit Parallel Bus. This line originates in pin 17 of bus expander IC8 and is coupled to Motherboard connector ST2 (pin45A) via bus driver IC23. During a WRITE control block (talk mode), microprocessor IC1 controls this line to remain low. During INTERROGATE control blocks (listen mode), IC1 controls this line to remain high.

The +15V DC lines provide power to all Buffer Stores connected to Bu2. Each Buffer Store should be equipped with an on board 5 volt regulator which supplies the controlled instruments.

The Ground lines provide the power return for all of the connected Buffer Stores. This ground should be connected to the Buffer Stores and to the controlled instruments.

Table 3.3.6 lists the actual connector pin number assignment.

Table 3.3.6 Control Expansion Connector pin number assignment for the Four Bit Parallel Bus

Signal Name	Pin		Signal Name
Data Output 2^0	1	13	Data Output 2^1
Data Output 2^2	2	14	Data Output 2^3
Data Position 2^0	3	15	Data Position 2^1
Data Position 2^2	4	16	$\overline{T}$/L ($\overline{Talk}$/Listen)
Address 2^0	5	17	Address 2^1
Address 2^2	6	18	Address 2^3
Listen 2^0	7	19	Listen 2^1
Listen 2^2	8	20	Listen 2^3
Data Position 2^3	9	21	NC
NC	10	22	$\overline{Remote}$/Local
+15V DC	11	23	Ground
+15V DC	12	24	Ground

3.3.7 Controlling Instruments on the Control Expansion Connector

Control Expansion connector BU2 allows the integration of fourteen additional instruments. Instruments connected to this port use Buffer Stores as the Four Bit Parallel interface and are controlled with a BCD parallel format. The address assignment for each additional instrument is set at the Buffer Store used by the individual instrument. Buffer Store address assignment must conform to table 3.1.2.

3.3.7.1 Writing to Instruments on the Control Expansion Connector

For the following discussion, refer to the IEEE-488 Interface Module schematic diagram. Microprocessor IC1 engages a talk mode sequence when it acknowledges a WRITE control block ("W _ _ _ _"). The steps taken by IC1 in the talk mode sequence are as follows;

1. Output binary 1110 (decimal 14) to port 5 of IC9. This is the reference Auxiliary Equipment Address utilized by the IEEE-488 firmware (see table 3.1.2).
2. Read 4-Bit Bus Auxiliary Equipment address byte and store it within IC1. Assignment of Buffer Store Auxiliary Equipment Address must conform to table 3.1.2.
3. Read first and last data position bytes, take the difference of their lower 4-bits and store the result within IC1 as variable COUNT. Also, set POSITION data variable to the value of the first data position byte (See table 3.3.2).
4. Write a 0 to pin 17 (P63) of IC8. This activates the talk mode in the 4-Bit Bus circuitry.
5. Read talk data byte and output its lower 4-bits to port 4 of IC8.
6. Output the four lower bits of POSITION data variable to port 7 of IC8.
7. Transfer the lower 4-bits of the 4-Bit Bus Auxiliary Equipment address byte read in steps 2 to port 5 of IC9; wait for 40 microseconds and then write 1110 (decimal 14) back to port 5 of IC9. The objective is to strobe the talk data into the addressed Buffer Store.
8. Decrease variable COUNT by one. If COUNT is not equal to zero, increment POSITION data variable and return to step number 5. If COUNT is equal to zero, the WRITE control block has ended.

   When a WRITE control block ends, IC1 looks for the next control block. The next control block could be a WRITE control block, an INTERROGATE control block (discussed below), or carriage return/line feed (CR/LF). When the next control block is CR/LF the IEEE-488 Interface module goes into idle condition.

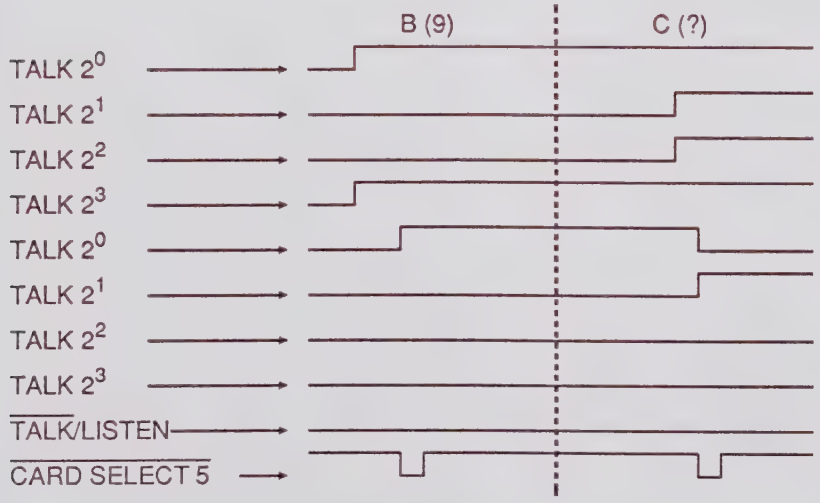


Figure 3.3.7.1 Transmission Sequence on the 4 Bit Parallel Bus in the Talk Mode

3.3.7.2 Interrogating Instruments on the Control Expansion Connector

For the following discussion, refer to the IEEE-488 Interface Module schematic diagram. The steps taken by microprocessor IC1 during an INTERROGATE control block ("I_ _ _) are the following:

1. Output binary 1110 (binary 14) to port 5 of IC9. This is the reference Auxiliary Equipment Address utilized by the IEEE-488 firmware (see table 3.1.2).
2. Read Auxiliary Equipment address byte and store within IC1. Assignment of Buffer Store Auxiliary Equipment Address must conform to table 3.1.2.
3. Read first and last position bytes, take the difference of their lower 4-bits and store the result as variable COUNT. Also, set POSITION data variable to the value of the first data position byte (see Table 3.3.2).
4. Write a binary 1 to pin 17 (P63) of IC8. This activates the listen mode in the 4-Bit Bus circuitry.
5. Write the lower 4-bits of POSITION data variable to port 7 of IC8.
6. Transfer the lower 4-bits of the Auxiliary Equipment address byte read in step 2 to port 5 of IC9; wait for 40 microseconds and then write 1110 (decimal 14) back to port 5 of IC9. The objective is to strobe the listen data from the addressed Buffer Store into the LISTEN DATA lines. The listen data is latched into bus expander IC8.
7. Read listen data from port 5 of IC8 and transfer the ASCII equivalent byte to the controller via @BU3. Since only four bits are read from port 5 of IC8, IC1 assembles the ASCII character by using the listen data for the lower 4-bits and attaching binary 0011 as the higher 4-bits. When byte transfer to the controller is complete, output binary 1110 (decimal 14) back to port 7 of IC9.
8. Decrease variable COUNT by one. If COUNT is not equal to zero, increment POSITION data variable and return to step 5. If count is equal to zero then go to idle condition.

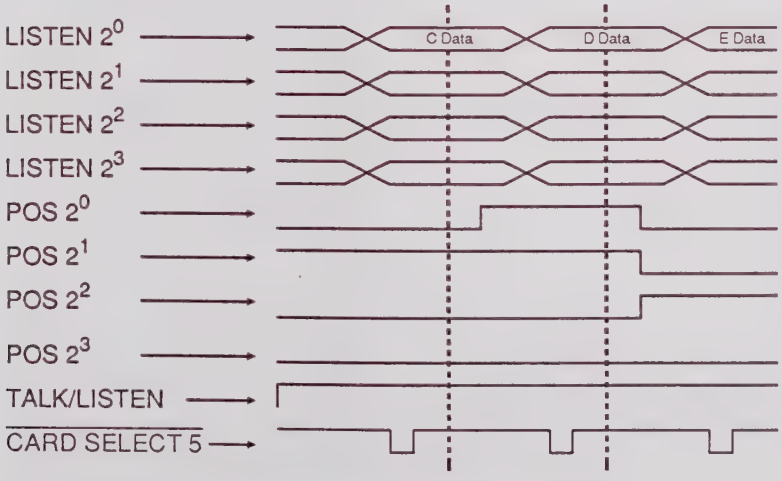
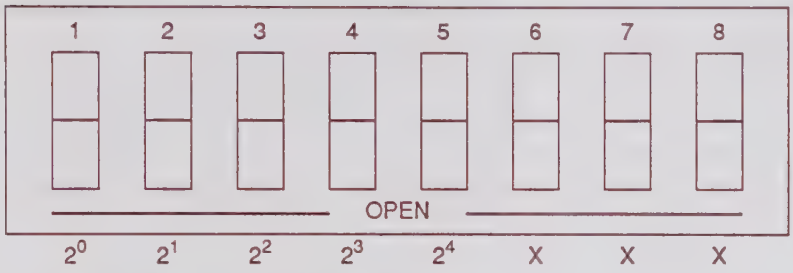


Figure 3.3.7.2 Transmission Sequence on the Four Bit Parallel Bus in the Listen (Interrogate) Mode

3.3.8 IEEE-488 Bus Address Switch

The IEEE-488 Interface Module address is programmed using switch SW1 positions one through five. Positions six through eight are don't cares. Therefore, the allowable addresses are any number between zero and thirty-one. Figure 3.3.9a shows a diagram of SW1.



X = Switch position does not matter

Figure 3.3.8a IEEE-488 Bus Address Switch (SW 1)

SW1 positions one through five enable setting the standard addresses 0 through 31. For example, programming decimal number 9 for the IEEE-488 Bus address is accomplished with the following settings:

Position 1 (2^0) = Closed (binary 1)
Position 2 (2^1) = Open (binary 0)
Position 3 (2^2) = Open (binary 0)
Position 4 (2^3) = Closed (binary 1)
Position 5 (2^4) = Open (binary 0)

Position 1 corresponds to the least significant bit and position 5 corresponds to the most significant bit.

Figure 3.3.8b shows a block diagram of the circuitry involved in the address recognition process. Once the address is set on switch SW1, the binary equivalent number is latched into IC11. This binary value is used by IC1 to determine if it is being addressed by the controller.

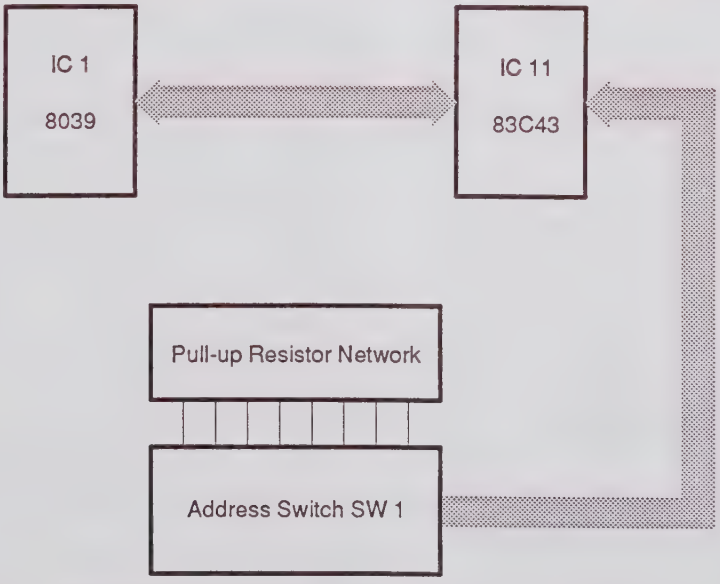


Figure 3.3.8b IEEE-488 Bus Address Switch circuit block diagram

3.3.9 Monitor LEDs

Four segment LED GL1 is used to provide visual indication of the bus status.

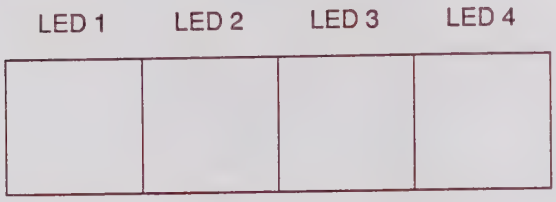


Figure 3.3.9a Monitor LEDs

Segment number one (LED 1) is the Power LED; it indicates that power is applied to the IEEE-488 Interface Module. This segment remains on as long as power is connected.

Segment number two (LED 2) is the Ready LED, it turns on when data is accepted by the IEEE-488 Interface Module.

Segment number three (LED 3)is the Listen (MLA) LED, it turns on when interrogate control blocks are sent to the IEEE-488 Interface Module.

Segment number four (LED 4) is the Talk (MTA) LED, it turns on when write control blocks are sent to the IEEE-488 Interface Module.

Figure 3.3.9b shows a block diagram of the Monitor LED circuitry. During IEEE-488 bus operations, microprocessor IC1 updates the status of the Monitor LEDs by writing the appropriate data into bus expander IC11.

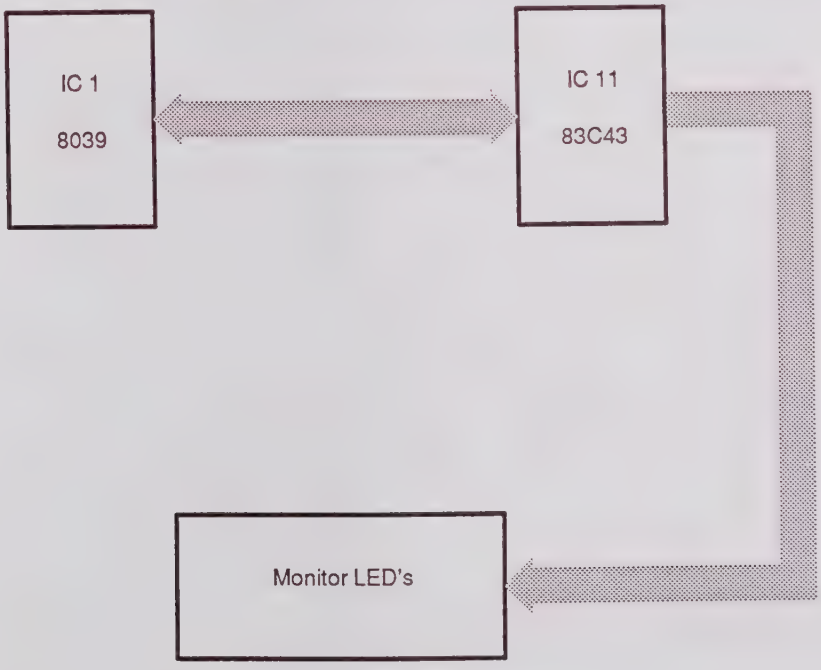


Figure 3.3.9b Monitor LEDs Circuitry Block Diagram

THIS DRAWING IS OUR PROPERTY;
IT IS NOT TO BE COPIED OR USED
WITHOUT THE WRITTEN CONSENT OF:
WANDEL & GOLTERMANN, INC.

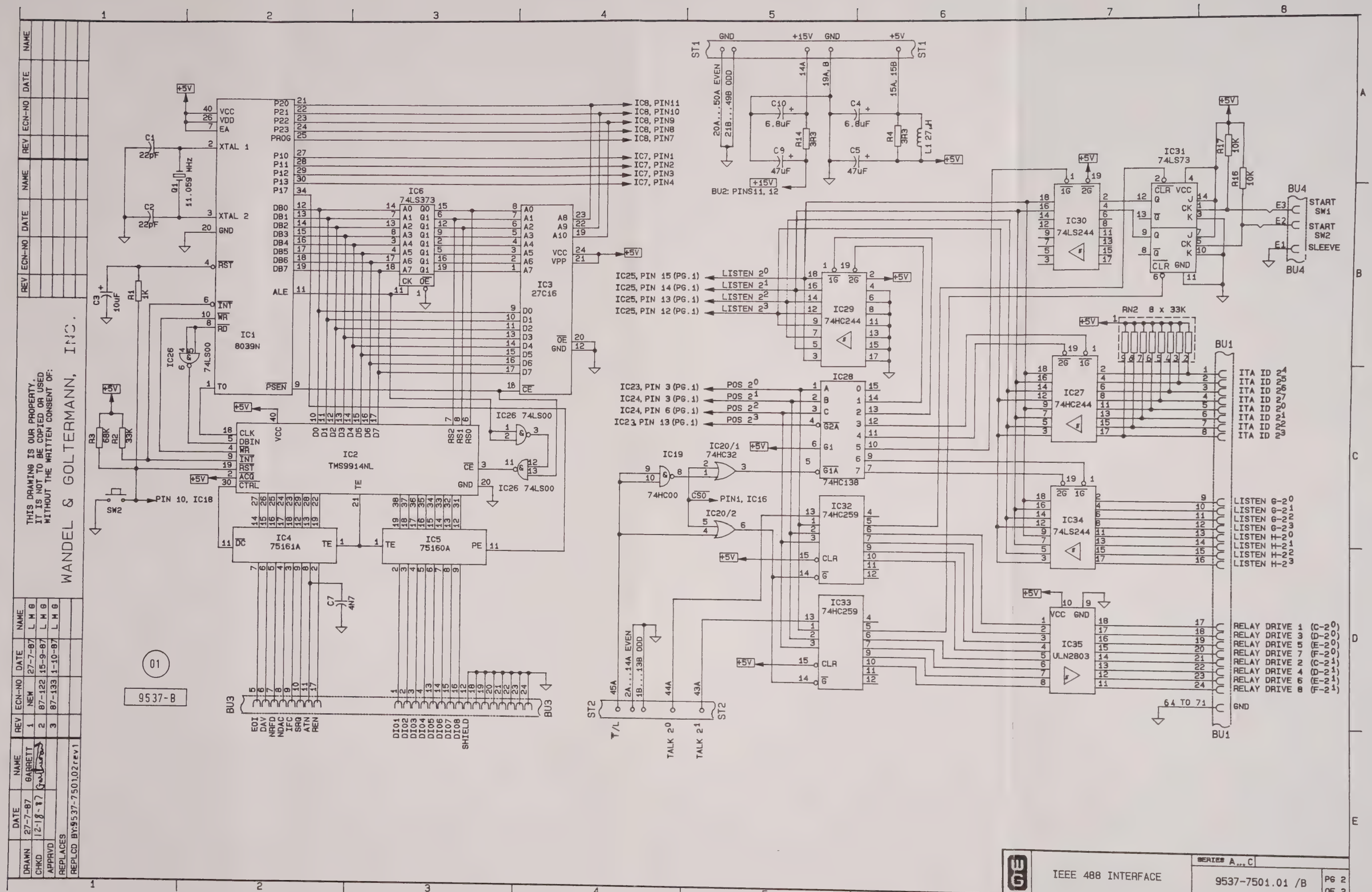
REV	ECN-NO	DATE	NAME
1	NEW	27-7-87	L M G
2	87-122	15-9-87	L M G
3	87-133	1-10-87	L M G

	NAME	DATE
DRAWN	BARRETT	27-7-87
CHKD		
APPRVD		
REPLACES		
REPLCD BY:9537-7501.02 rev1		

IC1, PIN21
IC1, PIN22
IC1, PIN23
IC1, PIN24
IC1, PIN25
IC1, PIN27
IC1, PIN28
IC1, PIN29
IC1, PIN30
IC7 74HC138
IC8 82C43
IC9 82C43
IC10 82C43
IC11 82C43
RN1 8 x 33K
SW1
GL1 HLMR 2820
R5 180R
R6 180R
R7 180R
R8 180R
R12 7K5
R14, C3* (PG 2)
TALK 2⁰/DIO 0
TALK 2¹/DIO 1
TALK 2²/DIO 2
TALK 2³/DIO 3
LISTEN 2⁰/DIO 4
LISTEN 2¹/DIO 5
LISTEN 2²/DIO 6
LISTEN 2³/DIO 7
IC12 CD4053 A
POS 2⁰/DAV
POS 2¹/NRFD
POS 2²/NDAC
POS 2³
T/L /EOI
IC17
IC18
74HC11
74HC02
IC21 74HC42
ADDR 2⁰/
ADDR 2¹
ADDR 2²
ADDR 2³
AUX/ MBUS
ATN
CLR
REMOTE/ LOCAL
IC13 74F241
IC14 74F241
IC15 74F241
BU2
IC22 74HC75
IC25 8286
IC16 74154
R10 21R5
C6 0.1uF
R11 100R
C8 0.01uF
IC19
74HC00
R13 5K1
IC23 8216
IC24 8216
DIEN
R15 10K
R1, R3, SW2 IC2, PIN19
IC29, PIN 18 (PG 2)
IC29, PIN 16 (PG 2)
IC29, PIN 14 (PG 2)
IC29, PIN 12 (PG 2)
ST2
PIN2, IC20
IC28, PIN 1 (PAGE 2)
IC28, PIN 4 (PAGE 2)
IC28, PIN 2 (PAGE 2)
IC28, PIN 3 (PAGE 2)
DAV /POS 2⁰
T/L/ EOI
ATN
POS 2³
POS 2¹/NRFD
POS 2²/NDAC
RESET
MBUS CLR
R/L
TRIG-1
TRIG-2
TALK 2⁰
TALK 2¹
TALK 2²
TALK 2³
LISTEN 2⁰
LISTEN 2¹
LISTEN 2²
LISTEN 2³
+15V
ADDR 2⁰
ADDR 2¹
ADDR 2²
ADDR 2³
POS 2⁰
POS 2¹
POS 2²
POS 2³
REM/LOCAL
T/L

01
9537-B

IEEE 488 INTERFACE	SERIES A...C	9537-7501.01 /B	PG 1 OF 2



THIS DRAWING IS OUR PROPERTY. IT IS NOT TO BE COPIED OR USED WITHOUT THE WRITTEN CONSENT OF:

WANDEL & GOLTERMANN, INC.

REV	ECN-NO	DATE	NAME
1	NEW	27-7-87	L M G
2	87-122	15-9-87	L M G
3	87-133	1-10-87	L M G

	DATE	NAME
DRAWN	27-7-87	GARRETT
CHKD	12-18-87	[signature]
APPRVD		
REPLACES		
REPLCD BY: 9537-7501.02 rev1		

IEEE 488 INTERFACE

SERIES A...C

9537-7501.01 /B

PG 2 OF 2

THIS DRAWING IS OUR PROPERTY.
IT IS NOT TO BE COPIED OR USED
WITHOUT THE WRITTEN CONSENT OF:
WANDEL & GOLTERMANN, INC.

REV	ECN-NO	DATE	NAME
1	87-199	17DEC87	L M G
2	88-004	18JAN88	L M G
3	88-073	25APR88	L M G

	DATE	NAME
DRAWN	27-7-87	GARRETT
CHKD		
APPRVD		

REPLACES: 9537-7501.01 REV3
REPLCD BY

IC1, PIN21
IC1, PIN22
IC1, PIN23
IC1, PIN24
IC1, PIN25
IC1, PIN27
IC1, PIN28
IC1, PIN29
IC1, PIN30
+5V
IC7 74HC138 (A0 A1 A2 G2A G2B G1 Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7)
IC8 82C43 (P20 P21 P22 P23 PROG P40 P41 P42 P43 P50 P51 P52 P53 P60 P61 P62 P63 P70 P71 P72 P73 CS DAV)
IC9 82C43
IC10 82C43
IC11 82C43
RN1 8 x 33K
SW1
GL1 HLMA 2820
R5 180R
R6 180R
R7 180R
R8 180R
IC12 CD4053 A (X0 X1 X)
R12 7K5
ADDR 2⁰/
ADDR 2¹/
ADDR 2²/
ADDR 2³/
AUX/ MBUS
ATN
IC21 74HC42 (A B C D Y1 Y2 Y3 Y4 Y5 Y6 Y7 Y8 Y9)
TALK 2⁰/DIO 0
TALK 2¹/DIO 1
TALK 2²/DIO 2
TALK 2³/DIO 3
LISTEN 2⁰/DIO 4
LISTEN 2¹/DIO 5
LISTEN 2²/DIO 6
LISTEN 2³/DIO 7
POS 2⁰/DAV
POS 2¹/NRFD
POS 2²/NDAC
POS 2³/
T/L /EOI
IC17
IC18
74HC11
74HC02
R11 100R
C8 0.01uF
IC19
74HC00
74HC00
IC22 74HC75 (1D 2D 3D 4D 1Q 2Q 3Q 4Q ENB ENB)
R10 21R5
C6 0.1uF
IC16 74154 (A B C D G1 G2)
CS0 PIN2, IC20
IC25 8286 (T/R OE)
IC29, PIN 18 (PG 2)
IC29, PIN 16 (PG 2)
IC29, PIN 14 (PG 2)
IC29, PIN 12 (PG 2)
ST2
R13 5K1
IC23 8216 (CS I0 I1 I2 I3 00 01 02 03 DIEN B0 B1 B2 B3)
IC24 8216 (CS I0 I1 I2 I3 00 01 02 03 DIEN B0 B1 B2 B3)
IC28, PIN 1 (PAGE 2)
IC28, PIN 4 (PAGE 2)
IC28, PIN 2 (PAGE 2)
IC28, PIN 3 (PAGE 2)
R15 10K
R1, R3, SW2
IC2, PIN19
CLR
REMOTE/ LOCAL
IC13 74F241
IC14 74F241
IC15 74F241
R14, C9+ (pg 2)
BU2
+15V
REM/ LOCAL T/L

ST2 pins:
44A 43A 42A 41A 44B 43B 42B 41B
40A 39A 38A 37A 36A 35A 34A 33A
40B 39B 38B 37B 36B 35B 34B 33B
CS1 CS2 CS3 CS4 CS5 CS6 CS7 CS8 CS9 CS10 CS11 CS12 CS13 CS14 CS15
50A DAV /POS 2⁰
45A T/L/ EOI
47A POS 2³
49A POS 2¹/NRFD
48A POS 2²/NDAC
49B RESET
46B MBUS CLR
13A TRIG-1
13B TRIG-2

TALK 2⁰ TALK 2¹ TALK 2² TALK 2³
LISTEN 2⁰ LISTEN 2¹ LISTEN 2² LISTEN 2³
ADDR 2⁰ ADDR 2¹ ADDR 2² ADDR 2³
POS 2⁰ POS 2¹ POS 2² POS 2³

01

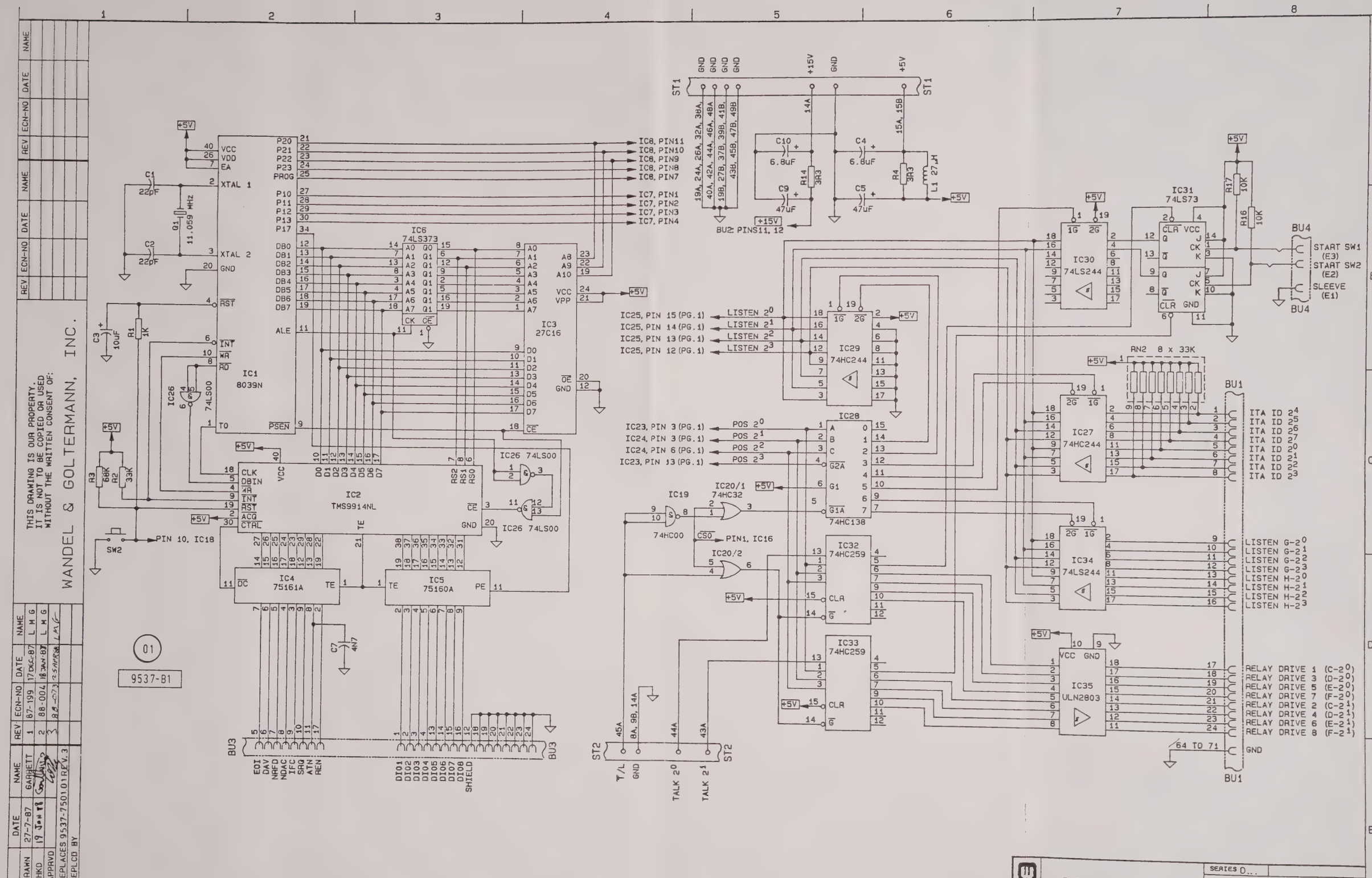
9537-B1

IEEE-488 INTERFACE

SERIES D...

9537-7501.02/B

PG 1 OF 2



THIS DRAWING IS OUR PROPERTY. IT IS NOT TO BE COPIED OR USED WITHOUT THE WRITTEN CONSENT OF:

WANDEL & GOLTERMANN, INC.

REV	ECN-NO	DATE	NAME
1	87-199	17 DEC-87	L M G
2	88-004	18 JAN-88	L M G
3	88-073	25 APR 88	LMG

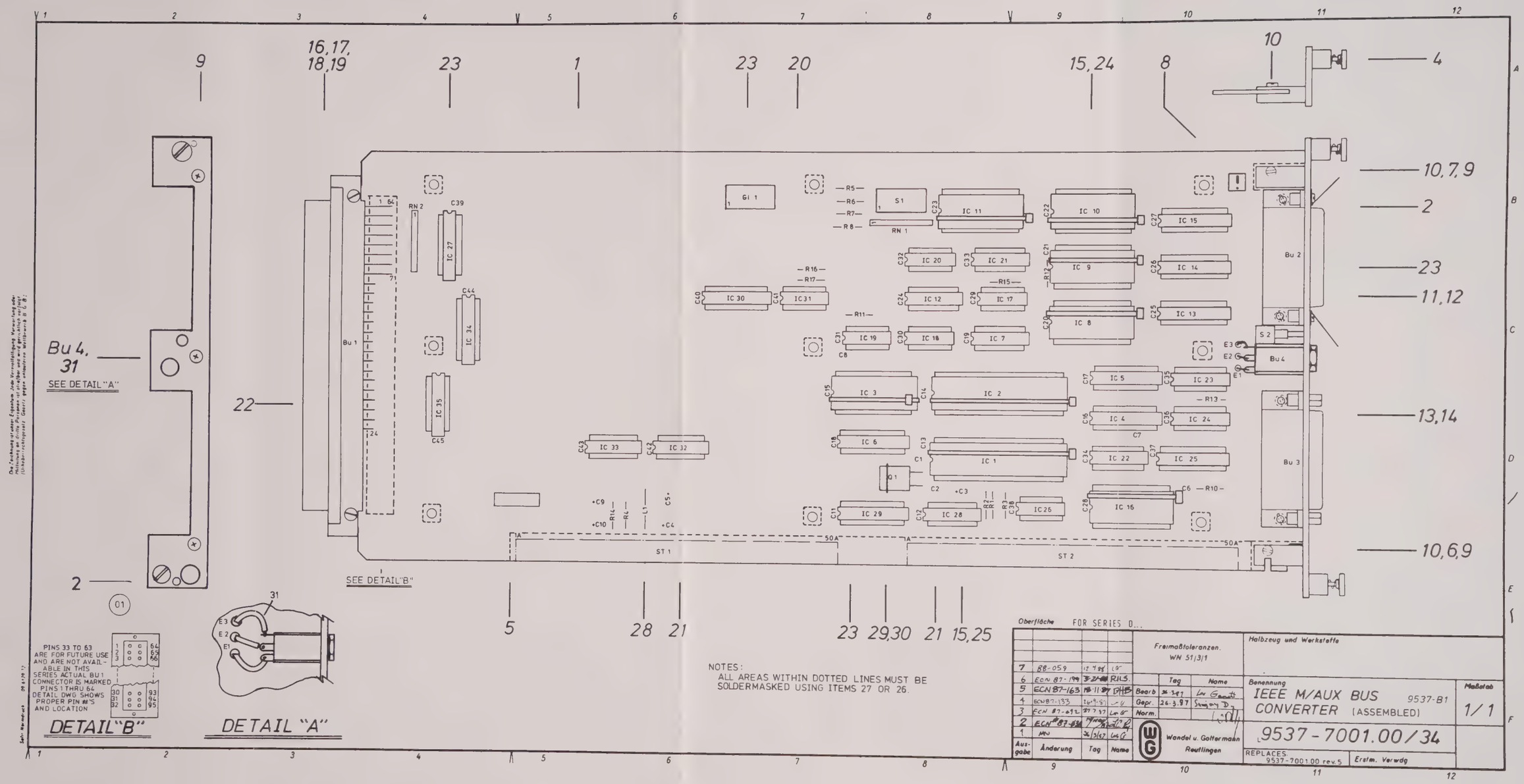
	DATE	NAME
DRAWN	27-7-87	GARRETT
CHKD	19 JAN 88	
APPRVD		
REPLACES 9537-7501.01 REV. 3		
REPLCD BY		

IEEE 488 INTERFACE

SERIES D...

9537-7501.~~01~~ 02 /B

PG 2 OF 2



NOTES:
ALL AREAS WITHIN DOTTED LINES MUST BE SOLDERMASKED USING ITEMS 27 OR 26.

Oberfläche FOR SERIES D...

Ausgabe	Änderung	Tag	Name
7	88-059	12.4.88	LG
6	ECN 87-199	3.2.88	RILS.
5	ECN 87-163	18.11.87	DHB
4	ECN 87-133	26.9.87	LG
3	ECN 87-092	27.7.87	LG
2	ECN 87-034	19/4/87	LG
1	MN	26/3/87	LG

Freimaßtoleranzen. WN 51/3/1

	Tag	Name
Bearb	26.3.87	Lu Gamott
Gepr.	26.3.87	Sanjay D
Norm.		

Wandel u. Gottermann Reutlingen

Halbzeug und Werkstoffe

Benennung
IEEE M/AUX BUS CONVERTER (ASSEMBLED) 9537-B1

Maßstab 1/1

9537-7001.00/34

REPLACES 9537-7001.00 rev.5

Erstm. Verwdg

WANDEL & GOLTERMANN TECHNOLOGIES, INC.

IEEE-488 INTERFACE MODULE

SERIES: ALL

BN 9537 ********** LIST OF REPLACEABLE PARTS ********** DATE: Jan 8, 1990

DIAG	REF	ITEM	QTY	PART NUMBER	DESCRIPTION	STOCK LOCATION	VERS/OPT	SERIES STRT	SERIES END	SUBASSEMBLY 9537-XXXX	SUBASSEMBLY CODE
							00 01			7001	S
		0	0	9537-7001.006	IEEE TO MAUX BUS CON		00 01			7001	A
		1	1	9537-7001.022	PC BOARD MACHINED		00 01			7001	
		3	1	9537-7001.051	PANEL REAR MARKED		00 01			7001	M
		5	1	0000-2911.029	LABEL SERIAL ABC		00 01			7001	
		6	1	9537-7001.064	BLOCK PANEL MTG 1		00 01			7001	
		7	2	9537-7001.080	BLOCK PANEL MTG 2		00 01			7001	
		8	1	0001-0072.468	LABEL YEL/BLK C-MOS		00 01			7001	
		13	2		STANDOFF HEX	XX24-0069.00	00 01			7001	
		15	8	0001-0035.214	TIE CABLE 1.5mm		00 01			7001	
		18	24		RECEPT PIN ANG ROW#1	XX03-0517.00	00 01			7001	
		19	8		RECEPT PIN ANG ROW#3	XX03-0518.00	00 01			7001	
		20	6	0000-7518.388	SOCKET IC DIP 14		00 01			7001	
		21	9	0000-7518.391	SOCKET IC 16 PIN DIP		00 01			7001	
		22	1	0000-7675.386	SOCKET IC DIP 18 .3"		00 01			7001	
		23	11	0000-7584.590	SOCKET IC DIP 20		00 01			7001	
		24	6	0000-7541.562	SOCKET IC DIL 24PIN		00 01			7001	
		25	2	0000-7541.711	SOCKET IC DIP 40		00 01			7001	
	BU	2	1		CONN M/R BALE RVF24P	XX03-0650.00	00 01			7001	
	BU	3	1		CONN M/R ANG REVF50P	XX03-0651.00	00 01			7001	
	BU	4	1		JACK PHONE 3C 4.5mm	XX03-0510.00	00 01			7001	
01	BU	1	1	9537-0000.101	CONN MODIFIED 64P		00 01			7001	M
01	C	1	1	0001-0004.287	C-CER 22P 2% NPO 63V		00 01			7001	
01	C	2	1	0001-0004.287	C-CER 22P 2% NPO 63V		00 01			7001	
01	C	3	1	0001-0040.885	C-ELYT TA 10U 20%25V		00 01			7001	
01	C	4	1		C-ELYT TA 6.8U10%35V	XX32-0086.00	00 01			7001	
01	C	5	1		C-ELYT TA 47u 10%20V	XX32-0096.00	00 01			7001	
01	C	6	1		C-CER 10 N 10% 50V	XX02-0270.00	00 01			7001	
01	C	7	1	0001-0004.795	C-CER 4.7N 10% 63V		00 01			7001	
01	C	8	1		C-CER 10 N 10% 50V	XX02-0270.00	00 01			7001	
01	C	9	1		C-ELYT TA 6.8U10%35V	XX32-0086.00	00 01			7001	
01	C	10	1		C-ELYT TA 6.8U10%35V	XX32-0086.00	00 01			7001	
01	C	11	1		C-CER 10 N 10% 50V	XX02-0270.00	00 01			7001	
01	C	12	1		C-CER 10 N 10% 50V	XX02-0270.00	00 01			7001	
01	C	13	1		C-CER 10 N 10% 50V	XX02-0270.00	00 01			7001	
01	C	14	1		C-CER 10 N 10% 50V	XX02-0270.00	00 01			7001	

WANDEL & GOLTERMANN TECHNOLOGIES, INC.

IEEE-488 INTERFACE MODULE

BN 9537 ********** LIST OF REPLACEABLE PARTS ********** SERIES: ALL DATE: Jan 8, 1990

DIAG	REF	ITEM	QTY	PART NUMBER	DESCRIPTION	STOCK LOCATION	VERS/OPT	SERIES STRT	SERIES END	SUBASSEMBLY 9537-XXXX	CODE
01	C	15	1		C-CER 10 N 10% 50V	XX02-0270.00	00 01			7001	
01	C	16	1		C-CER 10 N 10% 50V	XX02-0270.00	00 01			7001	
01	C	17	1		C-CER 10 N 10% 50V	XX02-0270.00	00 01			7001	
01	C	18	1		C-CER 10 N 10% 50V	XX02-0270.00	00 01			7001	
01	C	19	1		C-CER 10 N 10% 50V	XX02-0270.00	00 01			7001	
01	C	20	1		C-CER 10 N 10% 50V	XX02-0270.00	00 01			7001	
01	C	21	1		C-CER 10 N 10% 50V	XX02-0270.00	00 01			7001	
01	C	22	1		C-CER 10 N 10% 50V	XX02-0270.00	00 01			7001	
01	C	23	1		C-CER 10 N 10% 50V	XX02-0270.00	00 01			7001	
01	C	24	1		C-CER 10 N 10% 50V	XX02-0270.00	00 01			7001	
01	C	25	1		C-CER 10 N 10% 50V	XX02-0270.00	00 01			7001	
01	C	26	1		C-CER 10 N 10% 50V	XX02-0270.00	00 01			7001	
01	C	27	1		C-CER 10 N 10% 50V	XX02-0270.00	00 01			7001	
01	C	28	1		C-CER 10 N 10% 50V	XX02-0270.00	00 01			7001	
01	C	29	1		C-CER 10 N 10% 50V	XX02-0270.00	00 01			7001	
01	C	30	1		C-CER 10 N 10% 50V	XX02-0270.00	00 01			7001	
01	C	31	1		C-CER 10 N 10% 50V	XX02-0270.00	00 01			7001	
01	C	32	1		C-CER 10 N 10% 50V	XX02-0270.00	00 01			7001	
01	C	33	1		C-CER 10 N 10% 50V	XX02-0270.00	00 01			7001	
01	C	34	1		C-CER 10 N 10% 50V	XX02-0270.00	00 01			7001	
01	C	35	1		C-CER 10 N 10% 50V	XX02-0270.00	00 01			7001	
01	C	36	1		C-CER 10 N 10% 50V	XX02-0270.00	00 01			7001	
01	C	37	1		C-CER 10 N 10% 50V	XX02-0270.00	00 01			7001	
01	C	38	1		C-CER 10 N 10% 50V	XX02-0270.00	00 01			7001	
01	C	39	1		C-CER 10 N 10% 50V	XX02-0270.00	00 01			7001	
01	C	40	1		C-CER 10 N 10% 50V	XX02-0270.00	00 01			7001	
01	C	41	1		C-CER 10 N 10% 50V	XX02-0270.00	00 01			7001	
01	C	42	1		C-CER 10 N 10% 50V	XX02-0270.00	00 01			7001	
01	C	43	1		C-CER 10 N 10% 50V	XX02-0270.00	00 01			7001	
01	C	44	1		C-CER 10 N 10% 50V	XX02-0270.00	00 01			7001	
01	C	45	1		C-CER 10 N 10% 50V	XX02-0270.00	00 01			7001	
01	GL	1	1		LED LIGHT BAR GRN	XX37-0220.00	00 01			7001	
01	IC	1	1		IC UCOMPUT 8039 D40	XX35-0446.00	00 01			7001	
01	IC	2	1		IC GPIB TMS9914L D40	XX35-0445.00	00 01			7001	
01	IC	3	1	9524-9312.014	E-PROM PROGRMD M7042		00 01			7001	A
01	IC	4	1		IC 75161A	XX35-0442.00	00 01			7001	

WANDEL & GOLTERMANN TECHNOLOGIES, INC.

IEEE-488 INTERFACE MODULE

BN 9537 ********** LIST OF REPLACEABLE PARTS ********** SERIES: ALL DATE: Jan 8, 1990

DIAG	REF	ITEM	QTY	PART NUMBER	DESCRIPTION		STOCK LOCATION	VERS/OPT	SERIES STRT	SERIES END	SUBASSEMBLY 9537-XXXX CODE
01	IC	5	1		IC 75160A		XX35-0443.00	00 01			7001
01	IC	6	1	0001-0071.346	IC TTL 74LS373	D20		00 01			7001
01	IC	7	1	0000-7597.309	IC MOS 74HC138	D16		00 01			7001
01	IC	8	1		IC MOS 82C43	D24	XX35-0706.00	00 01			7001
01	IC	9	1		IC MOS 82C43	D24	XX35-0706.00	00 01			7001
01	IC	10	1		IC MOS 82C43	D24	XX35-0706.00	00 01			7001
01	IC	11	1		IC MOS 82C43	D24	XX35-0706.00	00 01			7001
01	IC	12	1		IC MOS 40532	D16	XX35-0188.00	00 01			7001
01	IC	13	1		IC TTL 74F241		XX35-0586.00	00 01			7001
01	IC	14	1		IC TTL 74F241		XX35-0586.00	00 01			7001
01	IC	15	1		IC TTL 74F241		XX35-0586.00	00 01			7001
01	IC	16	1	0001-0020.999	IC TTL 74154	D24		00 01			7001
01	IC	17	1	0000-7597.095	IC MOS 74HC02	D14		00 01			7001
01	IC	18	1	0000-7597.121	IC MOS 74HC11	D14		00 01			7001
01	IC	19	1	0000-7597.082	IC MOS 74HC00	D14		00 01			7001
01	IC	20	1	0000-7597.176	IC MOS 74HC32	D14		00 01			7001
01	IC	21	1	0000-7597.189	IC MOS 74HC42	D16		00 01			7001
01	IC	22	1	0000-7597.215	IC MOS 74HC75	D16		00 01			7001
01	IC	23	1		IC BUS/DRVR 8216	D16	XX35-0448.00	00 01			7001
01	IC	24	1		IC BUS/DRVR 8216	D16	XX35-0448.00	00 01			7001
01	IC	25	1		IC XCVR/8 8286	D20	XX35-0447.00	00 01			7001
01	IC	26	1	0000-7597.082	IC MOS 74HC00	D14		00 01			7001
01	IC	27	1	0000-7623.192	IC MOS 74HCT244	D20		00 01			7001
01	IC	28	1	0000-7597.309	IC MOS 74HC138	D16		00 01			7001
01	IC	29	1	0000-7623.192	IC MOS 74HCT244	D20		00 01			7001
01	IC	30	1	0000-7555.710	IC TTL 74LS244	D20		00 01			7001
01	IC	31	1		IC TTL 74LS73	D14	XX35-0260.00	00 01			7001
01	IC	32	1	0000-7597.590	IC MOS 74HC259	D16		00 01			7001
01	IC	33	1	0000-7597.590	IC MOS 74HC259	D16		00 01			7001
01	IC	34	1	0000-7555.710	IC TTL 74LS244	D20		00 01			7001
01	IC	35	1	0000-7579.657	IC DRVR ULN2803A	D18		00 01			7001
01	L	1	1	0001-0042.757	L-FERRITE 27U HORIZ			00 01			7001
01	Q	1	1		CRYSTAL 11.0592 MHz		XX16-0071.00	00 01			7001
01	R	1	1	0000-7585.544	R-MF 1K 1%	204		00 01			7001
01	R	2	1	0000-7607.383	R-MF 33K 1%	204		00 01			7001
01	R	3	1	0000-7607.257	R-MF 68.1K 1%	204		00 01			7001

WANDEL & GOLTERMANN TECHNOLOGIES, INC.

IEEE-488 INTERFACE MODULE

BN 9537 ********** LIST OF REPLACEABLE PARTS ********** SERIES: ALL DATE: Jan 8, 1990

DIAG	REF	ITEM	QTY	PART NUMBER	DESCRIPTION	STOCK LOCATION	VERS/OPT	SERIES STRT	SERIES END	SUBASSEMBLY 9537-XXXX	SUBASSEMBLY CODE
01	R	4	1	0000-7629.743	R-MF 3.32R 2% 204		00 01				7001
01	R	5	1	0000-7644.100	R-MF 178 OHM 1% 204		00 01				7001
01	R	6	1	0000-7644.100	R-MF 178 OHM 1% 204		00 01				7001
01	R	7	1	0000-7644.100	R-MF 178 OHM 1% 204		00 01				7001
01	R	8	1	0000-7644.100	R-MF 178 OHM 1% 204		00 01				7001
01	R	10	1	0000-7592.841	R-MF 21.5 OHM 1% 204		00 01				7001
01	R	11	1	0000-7519.471	R-MF 100 OHM 1% 204		00 01				7001
01	R	12	1	0000-7636.752	R-MF 7.5K 1% 204		00 01				7001
01	R	13	1	0000-7604.373	R-MF 5.11K 1% 204		00 01				7001
01	R	14	1	0000-7629.743	R-MF 3.32R 2% 204		00 01				7001
01	R	15	1	0000-7585.560	R-MF 10K 1% 204		00 01				7001
01	R	16	1	0000-7585.560	R-MF 10K 1% 204		00 01				7001
01	R	17	1	0000-7585.560	R-MF 10K 1% 204		00 01				7001
01	RN	1	1		NETWORK 9X33K	XX00-0697.00	00 01				7001
01	RN	2	1		NETWORK 9X33K	XX00-0697.00	00 01				7001
01	S	1	1	0000-7541.504	SW DIP 8SPST TOP D16		00 01				7001
01	S	2	1		SWITCH PB SPDT MOM	XX11-0082.00	00 01				7001

Digital Interface Module BN 9537/00.02

Contents **Page**

1. Introduction 1-1
2. Specifications 2-1
   - 2.1. DC Characteristics 2-1
   - 2.2. Input Signals (Transmit to UUT) 2-1
   - 2.3. Output Signals (Receive from UUT) 2-1
   - 2.4. Cables to the External System 2-1
3. Operating Description 3-1
   - 3.1. Detailed Description of Features 3-1
     - 3.1.1 Re-clocking of Input Signals 3-1
     - 3.1.2 24 Designated Parallel Input Signals (Transmit to UUT) 3-2
     - 3.1.3 4 Designated Input Clock Signals (Transmit to UUT) 3-3
     - 3.1.4 Output Signals (Receive from UUT) 3-4
     - 3.1.5 Computer Controlled External Start Signal 3-5
     - 3.1.6 Signal Flow Chart and Pin Locations 3-7
   - 3.2. Programming 3-11
     - 3.2.1 Programming Sheets 3-11
     - 3.2.2 Programming Description 3-17
       - 3.2.2.1 Programming Position A (Card Select) 3-17
       - 3.2.2.2 Programming Position B (Selecting the Overall Signal Path) 3-17
       - 3.2.2.3 Programming Positions C and D (Selecting 1 of 24 Designated Parallel Input Signals for Loop Back) 3-17
       - 3.2.2.4 Programming Position E (Completing the Loop Back Path for the 24 Parallel Input Signals) . . . 3-18
       - 3.2.2.5 Programming Position F (Looping Back 1 of 4 Designated Clock Input Signals) 3-18
       - 3.2.2.6 Programming Position G (Toggling the EXT STR Receive Line in the Loop Back Mode) 3-18
       - 3.2.2.7 Reading the Card ID 3-18
     - 3.2.3 Programming Example 3-19
   - 3.3. Circuit Description 3-21
     - 3.3.1 Four Bit Parallel Bus 3-21
     - 3.3.2 Re-clocking the Input Signals 3-21
     - 3.3.3 Input Signals (Transmit to UUT) 3-22
     - 3.3.4 Output Signals (Receive from UUT) 3-24
     - 3.3.5 External Start Signal 3-25
   - 3.4. Schematic Diagram / Parts List 3-27

Digital Interface Module Description and Operation

1. Introduction

The Digital Interface Module connects digital input and output signals between the test system and the unit under test. Up to 28 digital lines provide control signals and test stimulus to the Interchangeable Test Adapter (ITA) and the unit under test. Additionally, up to 17 digital lines provide digital responses from the Interchangeable Test Adapter (ITA) and unit under test to the test system.

2. Specifications

2.1. DC Characteristics

Maximum power consumption per module

	+5 V	+15 V	-15 V	Total
Current (Amps)	1.9	-----	-----	1.9
Power (Watts)	9.5	-----	-----	9.5

2.2. Input Signals (Transmit to UUT)

Number of digital input signals 28
Termination of input signals . . . . . 220Ω to 5V/330Ω to grnd
V in (high) . . . . . ≥2.0 volts
V in (low) . . . . . ≤0.8 volts
V in (maximum) . . . . . ≤7.0 volts
V out (high) . . . . . ≥2.0 volts @ 15ma
V out (low) . . . . . ≤0.55 volts @ 64ma
Frequency Range . . . . . DC to 10 MHz
Maximum re-clocking frequency . . . . . 30 MHz

2.3. Output Signals (Receive From UUT)

Number of digital output signals19
V in (high) . . . . . ≥2.0 volts
V in (low) . . . . . ≤0.8 volts
V in (maximum) . . . . . ≤7.0 volts
V out (high) . . . . . ≥2.0 volts @ 15ma
V out (low) . . . . . ≤0.55 volts @ 64ma
Frequency Range . . . . . DC to 10 MHz

2.4. Cables to External System

Number of cables needed 2
Cable type . . . . . 25 conductor, 93Ω, AMP coax

3. Operating Description

3.1. Detailed Description of Features

The Digital Interface Module has two basic features. Primarily, this module connects digital signals in both directions between the test system and the unit under test. Second, the transmitted digital signals can be looped back to the receive signal lines. This loop back feature allows the verification of the test system signals. The following block diagram shows the basic operation of this module.

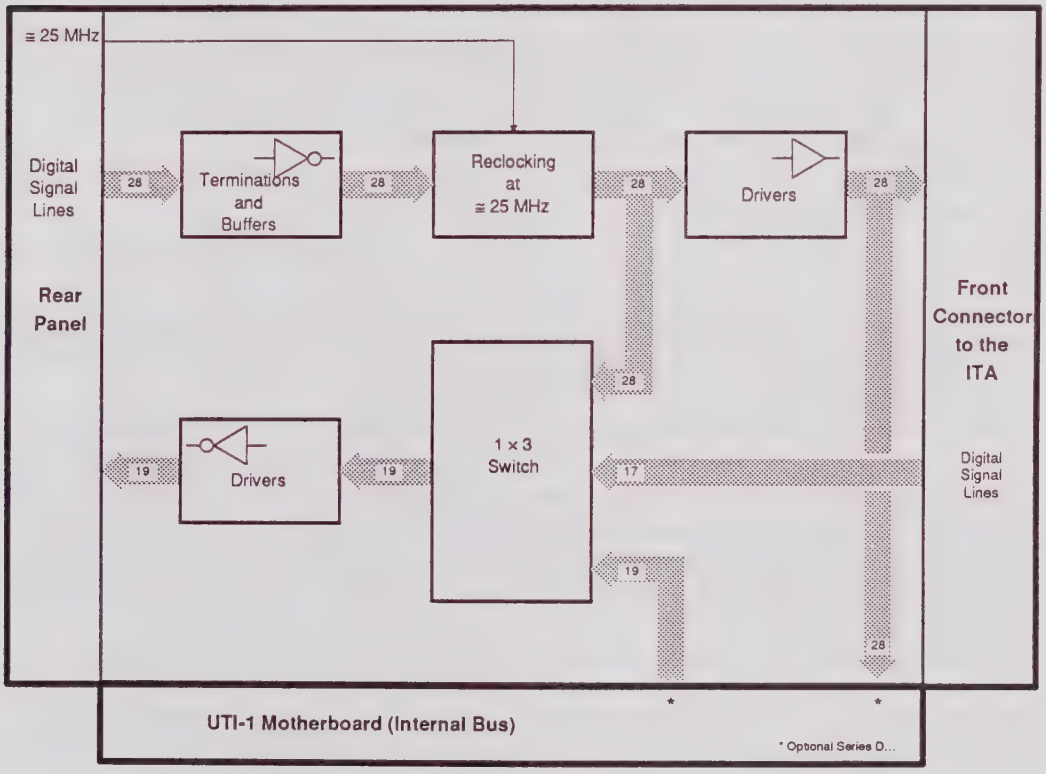


Figure 3.1. Digital Interface basic block diagram

In the following sections the digital signal lines will be discussed in groups based on their functions.

3.1.1 Re-clocking of the Digital Signals

All incoming digital signals from the test system are re-clocked with a signal at approximately 25 MHz. The actual re-clocking frequency must be a multiple of and phase locked to the incoming digital signals.

For best results, the ≅ 25 MHz incoming signal should be lined up with the incoming digital signal. This alignment is accomplished by moving a shorting plug between jumper positions 1 through 9. The digital signal is monitored at input pins 3, 4, 7, 8, 13, 14, 17, or 18 of IC 7, 8, 9, or 10 and compared to the clocking signal on pin 11 of these same ICs. Select a repetitive digital signal such as a clock for comparison. The falling edge of the re-clocking

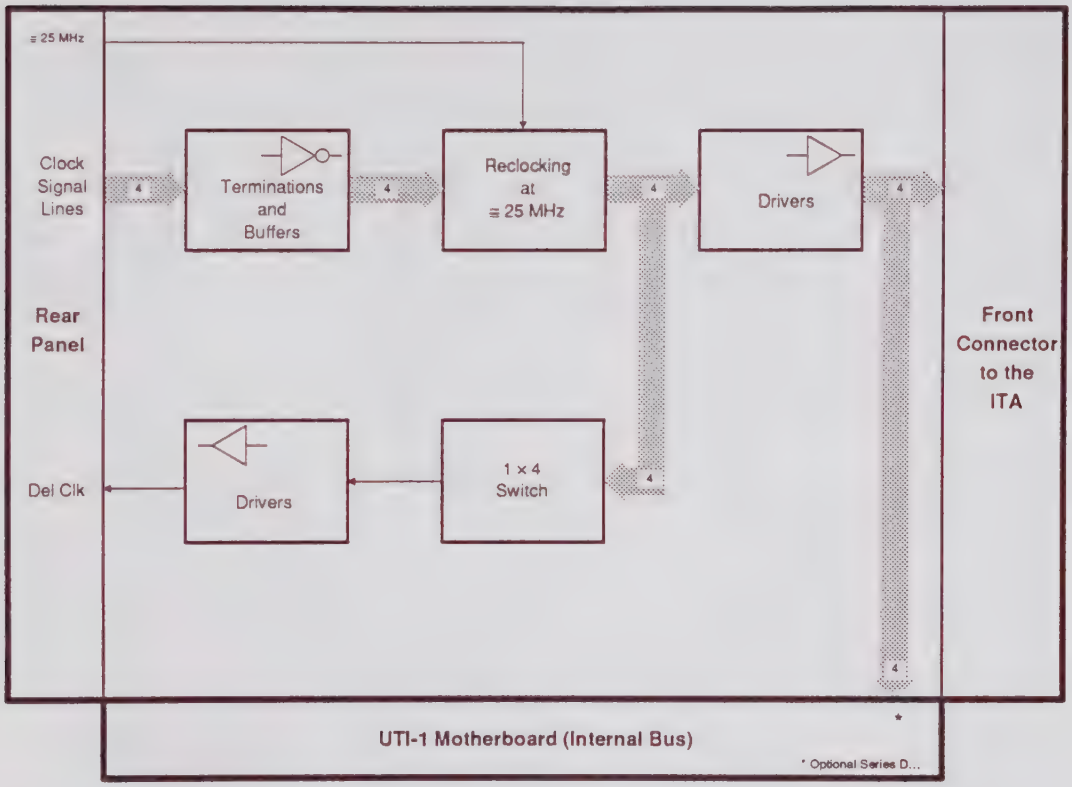


Figure 3.1.3 Clock Lines

3.1.4 Digital Signals from the ITA or Motherboard

Output signals originating at the Interchangeable Test Adapter (ITA) or the UTI-1 motherboard can be connected to the test system via the rear panel connector St4. The signal path is controlled by the operating program. Each of the incoming signals is terminated by 220Ω to +5 volts and 330Ω to ground on the Digital Interface Module. The incoming signals are connected to the line on the rear panel connector St4 of the same name. The resulting signal on the rear panel connector is the inverse of the original signal.

Seventeen signal lines are connected to the test system from the front connector Bu1 and nineteen signal lines are connected to the test system from the motherboard.

The common signal lines from both the ITA connection and the motherboard are:

REC-B, REC-C, REC-D, REC-E, REC-F, REC-G, REC-J, REC-K, REC-L, REC-M, REC-N, REC-P, DEL CK, EXT STR, DEL STB, SHIFT, and SF.

The two additional lines from the motherboard are FIX CK and FIX STB. When using these lines, jumpers E1-E2 and E3-E4 must be installed.

See the schematic diagram for the location of each of these lines.

Note: The motherboard connections are standard in Series A through C and optional in Series D and up.

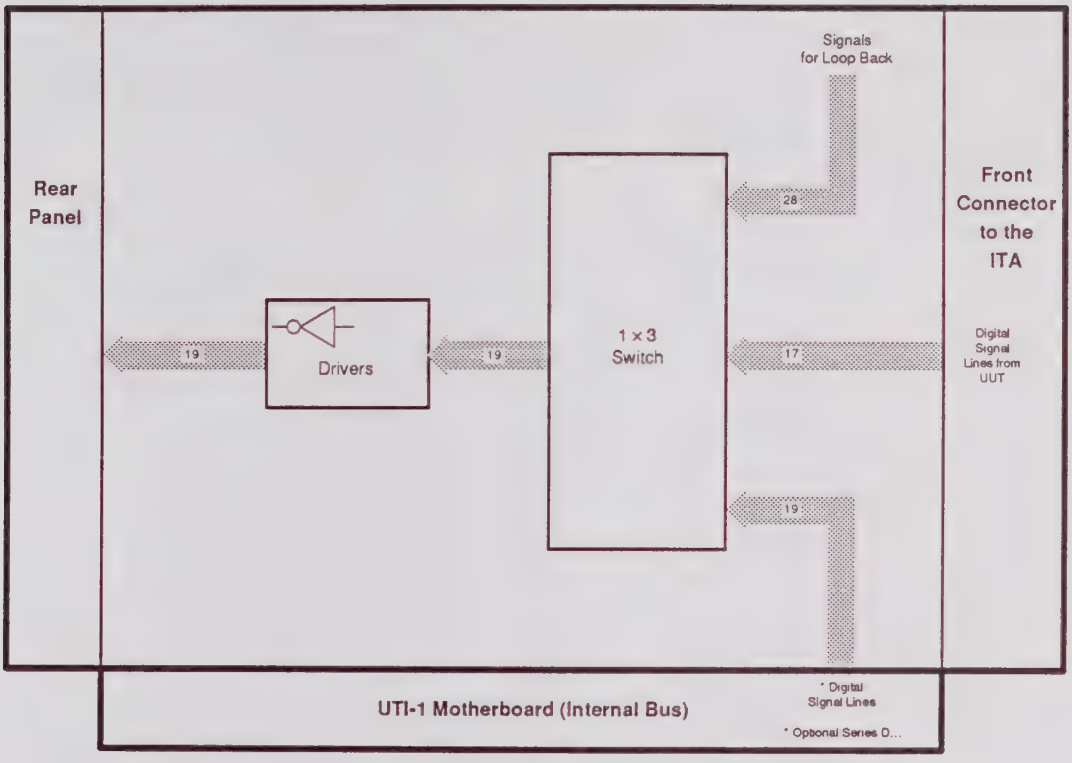


Figure 3.1.4 Output Digital Signals to the Test System

3.1.5 Computer Controlled External Start Signal

When the module is set to the loop back mode, the EXT STR line on the rear panel can be set to low or high by programming a "1" or "0" respectively in the G program position. See the programming section 3.2. for more information on programming this function.

3.1.6 Signal Flow Chart and Pin Locations

Signal Name	Rear Panel Connector	Signal Direction	Front Connector (to ITA) Bu1	Motherboard Connection (Note 1)	Notes
25 MHz	ST3 pin 1				Reclocking signal input
B-1	ST3 pin 2	→	2	ST1 pin 20B	
C-1	ST3 pin 3	→	3	ST1 pin 21A	
D-1	ST3 pin 4	→	4	ST1 pin 22B	
E-1	ST3 pin 5	→	6	ST1 pin 23A	
F-1	ST3 pin 6	→	7	ST1 pin 24B	
G-1	ST3 pin 7	→	8	ST1 pin 25A	
J-1	ST3 pin 8	→	65	ST1 pin 26B	
K-1	ST3 pin 9	→	66	ST1 pin 27A	
L-1	ST3 pin 10	→	67	ST1 pin 28B	
M-1	ST3 pin 11	→	69	ST1 pin 29A	
N-1	ST3 pin 12	→	70	ST1 pin 30B	
P-1	ST3 pin 13	→	71	ST1 pin 31A	
B-2	ST3 pin 14	→	10	ST1 pin 32B	
C-2	ST3 pin 15	→	11	ST1 pin 33A	
D-2	ST3 pin 16	→	12	ST1 pin 34B	
E-2	ST3 pin 17	→	14	ST1 pin 35A	
F-2	ST3 pin 18	→	15	ST1 pin 36B	
J-2	ST3 pin 19	→	73	ST1 pin 37A	
K-2	ST3 pin 20	→	74	ST1 pin 38B	
L-2	ST3 pin 21	→	75	ST1 pin 39A	
M-2	ST3 pin 22	→	77	ST1 pin 40B	
N-2	ST3 pin 23	→	78	ST1 pin 41A	
P-2	ST3 pin 24	→	79	ST1 pin 42B	
Ser PCM	ST3 pin 25	→	16	ST1 pin 43A	

Signal Name	Rear Panel Connector	Signal Direction	Front Connector (to ITA) Bu1	Motherboard Connection (Note 1)	Notes
CK-1	ST4 pin 15	→	18	ST1 pin 44B	
CK-2	ST4 pin 16	→	19	ST1 pin 45A	
CK-3	ST4 pin 17	→	81	ST1 pin 46B	
CK-4	ST4 pin 18	→	82	ST1 pin 47A	
REC-B	ST4 pin 2	←	21	ST1 pin 48B	
REC-C	ST4 pin 3	←	22	ST1 pin 49A	
REC-D	ST4 pin 4	←	23	ST1 pin 50B	
REC-E	ST4 pin 5	←	25	ST2 pin 1A	
REC-F	ST4 pin 6	←	26	ST2 pin 2B	
REC-G	ST4 pin 7	←	27	ST2 pin 3A	
REC-J	ST4 pin 8	←	84	ST2 pin 4B	
REC-K	ST4 pin 9	←	85	ST2 pin 5A	
REC-L	ST4 pin 10	←	86	ST2 pin 6B	
REC-M	ST4 pin 11	←	88	ST2 pin 7A	
REC-N	ST4 pin 12	←	89	ST2 pin 8B	
REC-P	ST4 pin 13	←	90	ST2 pin 9A	
DEL CK	ST4 pin 20	←	29	ST2 pin 10B	
EXT STR	ST4 pin 21	←	92	ST2 pin 11A	
DEL STB	ST4 pin 22	←	30	ST2 pin 12B	
SHIFT CLK	ST4 pin 23	←	31	ST2 pin 13A	
$\overline{SF}$	ST4 pin 24	←	93	ST2 pin 14B	
FIX CK	ST4 pin 1	←		ST2 pin 29A	
FIX STB	ST4 pin 19	←		ST2 pin 29B	

3.2. Programming

3.2.1 Programming Sheets

Function	A	B	C	D	E	F	G
Card Select (Note 1)	X						
Enable Receive from Motherboard (Note 2)		0					
Disable Receive from Motherboard (Note 2)		1					
Loop Back Testing		3					
Enable Receive from Front Panel		5					
Disable Transmit to Motherboard and Front Panel		8					
Connect B-1 for Loop Back			1	0			
Connect C-1 for Loop Back			1	1			
Connect D-1 for Loop Back			1	2			
Connect E-1 for Loop Back			1	3			
Connect F-1 for Loop Back			1	4			
Connect G-1 for Loop Back			1	5			
Connect J-1 for Loop Back			1	6			
Connect K-1 for Loop Back			1	7			
Connect L-1 for Loop Back			2	0			
Connect M-1 for Loop Back			2	1			
Connect N-1 for Loop Back			2	2			
Connect P-1 for Loop Back			2	3			

Notes:

1) X = the slot number where the module is installed.
2) The Motherboard connections are standard in Series A through C, and optional in Series D and up.

Function	A	B	C	D	E	F	G
Card Select (Note 1)	X						
Connect B-2 for Loop Back			2	4			
Connect C-2 for Loop Back			2	5			
Connect D-2 for Loop Back			2	6			
Connect E-2 for Loop Back			2	7			
Connect F-2 for Loop Back			3	0			
Connect J-2 for Loop Back			3	1			
Connect K-2 for Loop Back			3	2			
Connect L-2 for Loop Back			3	3			
Connect M-2 for Loop Back			3	4			
Connect N-2 for Loop Back			3	5			
Connect P-2 for Loop Back			3	6			
Connect Serial PCM for Loop Back			3	7			
Enable REC-C for Loop Back					0		
Enable REC-B, D, E, and F for Loop Back					1		
Enable REC-G, J, K, and L for Loop Back					2		
Enable REC-M, N, and P for Loop Back					3		

Notes:

1) X = the slot number where the module is installed.

Function	A	B	C	D	E	F	G
Card Select (Note 1)	X						
Connect Clk-1 for Loop Back						0	
Connect Clk-2 for Loop Back						1	
Connect Clk-3 for Loop Back						2	
Connect Clk-4 for Loop Back						3	
External Start High (for Loop Back Only) Note 2							0
External Start Low (for Loop Back Only) Note 2							1

Notes:

1) X = the slot number where the module is installed.
2) When used in an AMS-964 system, the levels are reversed due to inverters in the Active Interfaces.

3.2.2 Programming Description

The programming word for the Digital Interface Module contains 7 positions (A through G) and each position has sixteen possible values. These values are 0 through 9 and the ASCII characters :, ;, <, =, >, and ?, which are equivalent to the decimal numbers 10, 11, 12, 13, 14, and 15 respectively.

3.2.2.1 Programming Position A (Card Select)

Position A is used to select the proper module in the UTI-1. The value used in this position depends on which slot the Digital Interface Module is in. When looking at the rear of the UTI-1, slot 0 is the most right slot and slot 15 is the most left slot. Position A must be programmed whenever you wish to program any element on this module. If you do not program this position, the information will never reach this module.

Note: The card select data in position A is latched in the computer interface module. Once the data in this position is sent, the computer interface module will continue to send the proper card select pulse with every OUTPUT statement; therefore, new card select data need only be sent when writing to a different module.

3.2.2.2 Programming Position B (Selecting the Overall Signal Path)

When a "0" is programmed in this position, the received data from the motherboard is connected to the rear panel test system connections.

When a "1" is programmed in this position, the received data path from the motherboard to the rear panel test system connections is disabled.

When a "3" is programmed in this position, the signal path to loop back transmitted signals to receive signal lines is enabled, and the receive paths from both the motherboard and front panel are disabled. Additionally, the input signal from the test system labelled G-1 is looped back to both the DEL STB and SHIFT CLOCK lines. In order to complete other loop back paths, positions C, D, E, F, and/or G must be programmed.

When a "5" is programmed in this position, the received data path from the front panel is enabled and the path from the motherboard is disabled. When a "8" is programmed in this position the transmit data path to the motherboard and front panel is disabled.

Note: The motherboard connections to and from the motherboard are optional in series D and up.

3.2.2.3 Programming Positions C and D (Selecting one of the 24 Designated Parallel Input Signals for Loop Back)

In addition to programming a "3" in position B, programming positions C and D connects to the loop back path any one of 24 input digital signals. These signals can be looped back to the lines marked REC by programming position E. See the programming chart for the specific lines involved.

3.2.2.4 Programming Position E (Completing the Loop Back Path for the 24 Designated Parallel Input Signals)

In addition to programming a "3" in position B and programming positions C and D, position E completes the loop back path to groups of lines marked REC. Any one of the 24 rear panel input signals can be connected to groups of the rear panel lines marked REC. See the programming chart for the specific lines in each group and the program characters used.

3.2.2.5 Programming Position F (Looping Back One of the 4 Designated Clock Input Signals)

In addition to programming a "3" in position B, position F completes the loop back path for four of the rear panel input signals marked CLK to the rear panel output line marked DEL CK. See the programming chart for the names of the specific lines and the program characters used.

3.2.2.6 Programming Position G (Toggling the EXT STR Receive Line in the Loop Back Mode)

In addition to programming a "3" in position B, position G to a "0" or "1" sets the rear panel output line marked EXT STR to a high (5 volts) or a low (0 volts) respectively.

3.2.2.7 Reading the Card ID

The card ID number can be read back from positions B & C. Since binary number 2^0, 2^1, 2^2 and 2^3 are read back in data position C and binary numbers 2^4, 2^5, 2^6 and 2^7 are read back in data position B, the information in M$ must be converted to a decimal ID number. Since the ASCII characters in each position represent 0 through 15, the result can be treated as a HEX number. In the case of this module the card ID in HEX and decimal is "02".

Note: The actual characters read back in each data position will be the ASCII characters 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, :, ;, <, =, >, and ? which correspond to the HEX characters 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, and F respectively.

The identification number is read back in the following manner:

1. UTI-1 IEEE-488 bus address = 709, 4 Bit Parallel Bus Address = 1, Card slot = 1.
2. Send the card select number and the command to interrogate positions B and C ("I" control block for listen operation):

   OUTPUT 709;"W1AA1" & "I1BC"

   The first portion of the output statement, "W1AA1" is a talk operation to select the card slot position of the module (A = 1). The second portion, "I1BC", is a listen operation which interrogates positions B and C of the selected card slot. The output statement can also be written as OUTPUT 709;"W1AA1I1BC".
3. Read back the information from the IEEE-488 bus and assign it to a string variable.

   ENTER 709;Result$

3.2.3 Programming Example

The following example shows how a programming word may be built using the IEEE-488 Bus Interface and HP 200 or 300 series computer. Please refer to the programming sheets.

In the Digital Interface Module, a control word consists of: "W$x S_1 S_2$abcdefg"

"x" is the 4 Bit Parallel Bus address for the UTI-1 mainframe. This address is always "1".

"$S_1 S_2$ are the position selector; i.e. for positions A through G, S_1 = A and S_2 = G.

"a" is the card slot select address.

"b through g" are control data values.

Suppose the user had the following configuration requirements:

1) The UTI-1 IEEE-488 bus address = 709, the Four Bit Parallel Bus address for UTI-1 modules = 1, and the card slot select address = 1. The output statement thus far is:

   OUTPUT 709;"W1AA1"

2) Set up module for loop back testing (B = 3). The output statement thus far is:

   OUTPUT 709;"W1AB13"

3) Connect rear panel input line M-2 for loop back (C = 3, D = 4). The output statement thus far is:

   OUTPUT 709;"W1AD1334"

4) Connect rear panel input line M-2 to rear panel output lines REC-G, REC-J, REC-K, and REC-L (E = 2). The output statement thus far is:

   OUTPUT 709;"W1AE13342"

5) Connect rear panel input line CLK-1 to rear panel output line DEL CK (F = 0). The output statement thus far is:

   OUTPUT 709;"W1AF133420"

6) Set rear panel output line EXT STR to high (G = 0). The final output statement is:

   OUTPUT 709;"W1AG1334200"

3.3. Circuit Description

3.3.1 Four Bit Parallel Bus

The $\overline{CS}$ ($\overline{Card\ Select}$) input line on St2 pin 50B must be in the low state (0 volts) in order for any communication to occur between the system controller and this module. A 0 volt pulse will occur at this point for each data position that is written to or interrogated. This occurs only when the proper number, corresponding to the UTI-1 slot number, is sent in the A position. See section 3.2. for further programming information.

In order for the addressable latch IC's (IC35, IC36, IC37, IC 38) to pass any talk information, the card select low pulse must be felt at pin 14 of each of these IC's. The signal path is IC 33 pin 4 to 6 and IC33 pin 10 to 8. This signal will be passed through IC33 pin 10 when the $\overline{T}$/L ($\overline{talk}$ / listen) pin is low, indicating the talk mode. If a high is on the $\overline{T}$/L line, indicating the listen mode, the card select signal will be blocked at IC33 pin 10.

When the $\overline{T}$/L pin is high, the card select will be passed through IC33 pins 13 and 11. The addressable latch IC39 will be activated by the card select when the POS 2^3 line is low. This activates the latch connected to the listen ports.

Each of the talk latches, IC35, IC36, IC37, and IC38, represents a BCD number. IC35 is for 2^0 or 1; IC36 is for 2^1 or 2; IC37 is for 2^2 or 4; IC38 is for 2^3 or 8. The talk data lines from St2 are connected to pin 13 of the appropriate ICs. This data will be latched to the appropriate output pin. The signals labeled POS 2^0, POS 2^1, and POS 2^2 will determine which data is latched to which output. The following chart will show the relationship between the position and the corresponding output pin.

POS 2^0	POS 2^1	POS 2^2	Output pin	Position
L	L	L	4	A
H	L	L	5	B
L	H	L	6	C
H	H	L	7	D
L	L	H	9	E
H	L	H	10	F
L	H	H	11	G
H	H	H	12	H

Each of the latched outputs are used to activate different signal paths.

The Listen lines are used to read the card ID. This ID code is generated by IC40. When a low pulse is on pin 19, the MSB nibble corresponding to the ground on pins 11, 13, 15, and 17 is selected. This code will be read by the computer as a 0 in the B position. When a low pulse is on pin 1, the LSB nibble corresponding to the ground on pins 8, 6, and 2 and the +5V on pin 4 is selected. This code will be read by the computer as a 2 in the C position.

3.3.2 Re-clocking of Input Signals

After the incoming signals from the test system are buffered by IC 3, IC 4, IC 5, and IC 6, they are re-clocked at IC 7, IC 8, IC 9, and IC 10. The 25 MHz re-clocking signal at St 3 pin 1 should be a multiple of and phase locked to the frequency of the incoming digital signals. The re-clocking signal passes through a series of NAND gates located in IC 1 and IC 2. The number of gates this signal passes through is controlled by the jumper on placed on pin positions 1, 2, 3, 4, 5, 6, 7, 8, or 9. By placing the jumper on different positions, the delay of the re-clocking signal is controlled. The leading edge of the re-clocking signal on pin 11 of

IC 7 through IC 10 gates the incoming signals on pins 3, 4, 7, 8, 13, 14, 17, and 18 to the respective output pins.

For best operation, the falling edge of the re-clocking signal should line up with the positive or negative transitions of the incoming digital signal. Deviations of more than 5nsec may cause an excessive loss of signal shape and possible loss of data bits. For a description of setting the delay of the re-clocking signal, see section 3.1.1.

3.3.3 Input Signals (Transmit to UUT)

Each of these signal lines are terminated by 220Ω to +5 volts and 330Ω to ground. These termination networks are shown on the schematic as a "T".

After the input signals are inverted by buffers IC 3 through IC 6, they are re-clocked at IC 7 through 10 to the output drivers IC 11 through IC 18. A high on pin 19 and a low on pin 1 of the driver ICs will pass the signals to the output pins. The output pins of IC 11, IC 13, IC 15, and IC 17 are connected to the motherboard connections on St 1. These ICs and connections are standard on series A through C and optional on series D and up. The output pins of IC 12, IC 14, IC 16, and IC 18 are connected to the Interchangeable Test Adapter connections on Bu 1.

Enabling and Disabling the Output Driver ICs

In order for the output drivers to be enabled, an "8" must not be programmed in the B data position. This will ensure a low on pin 5 of IC 38. This low is connected to IC 25 pin 8 and pin 1 ($\overline{1G}$) of the driver ICs. Since IC 25 is an invertor, the output pin 12 is high and connected to pin 19 (2G) of the driver ICs. The low on the $\overline{1G}$ pins and the high on the 2G pins will enable the driver ICs and the data on their inputs will be passed to the outputs.

In order for the output drivers to be disabled, an "8" must be programmed in the B data position. This will put a high on pin 5 of IC 38. This high is connected to IC 25 pin 8 and pin 1 ($\overline{1G}$) of the driver ICs. Since IC 25 is an inverter, the output pin 12 is low and connected to pin 19 (2G) of the driver ICs. The high on the $\overline{1G}$ pins and the low on the 2G pins will disable the driver ICs and keep their output pins at a high impedance.

Looping Back the 24 Designated Parallel Input Signals

Looping back the 24 input signals described in section 3.1.2 is accomplished by programming data positions B, C, D, and E.

When a "3" is programmed in the B position for loop back testing, a high is on IC 35 pin 5 and IC 36 pin 5. The high on IC 35 pin 5 is connected to IC 26 pin 19, and IC 19 through 22 pins 1 and 19. The drivers IC 19, IC 20, IC 21, IC 22, and half of IC 23 will be disabled and their output pins will be at a high impedance. The high on IC36 pin 5 is connected to IC 25 pin 4. Since IC 25 is an inverter, IC 25 pin 16 will be low. IC 25 pin 16 is connected to IC 25 pin 19 and IC 32 pin 1. The low on IC 25 pin 19 activates the drivers connected to output pins 9, 7, 5, and 3. The low on IC 32 pin 1 activates the first half of this decoder/demultiplexer. Since IC 32 pin 15 is connected to ground the second half of this IC is always activated.

In order to loop back one specific input signal, data position C and D must be programmed. IC 35 pin 6 is the talk 2^0 data for position C and is connected to IC 32 pin 14. IC 36 pin 6 is the talk 2^1 data for position C and is connected to IC 32 pin 13. Therefore, the data entered in data position C will cause one of the output pins to a low state. If a "1" is programmed, output pin 11 will be low and IC 27 will be activated. If a "2" is programmed, output pin 10

will be low and IC 28 will be activated. If a "3" is programmed, output pin 9 will be low and IC 29 will be activated. The position D talk 2^0, 2^1, and 2^2 data from IC 35 pin 7, IC 36 pin 7, and IC 37 pin 7 respectively are connected to the select inputs of the 8 input multiplexer ICs (IC 27, IC 28, and IC 29). The talk data in position D selects which input line connects to output pin 5 of the selected multiplexer IC. The input lines of IC 27, IC 28, and IC 29 are connected to 24 of the incoming signals after they have been re-clocked. The output pins of IC 27, IC 28, and IC 29 connect to the input pins of IC 23 and IC 24 through the OR gates of IC 31.

Once the card has been set for loop back by programming data position B and one of the 24 input lines has been selected for loop back by programming data positions C and D, the REC output line or group of lines the input line is looped back to must be selected by programming position E. The position E talk 2^0 and 2^1 data from IC 35 pin 9 and IC 36 pin 9, respectively, is connected to IC 32 pins 2 and 3. Therefore, the data entered in data position E will cause one of the output pins to a low state. If a "0" is programmed, output pin 4 will be low and the first half of IC 23 will be activated. If a "1" is programmed, output pin 5 will be low and the other half of IC 23 will be activated. If a "2" is programmed, output pin 6 will be low and the first half of IC 24 will be activated. If a "3" is programmed, output pin 7 will be low and the other half of IC 24 will be activated. If the first half of IC 23 is activated the selected incoming signal will be connected to the REC-C output line. If the second half of IC 23 is activated, the selected incoming signal will be connected to the REC-B, REC-D, REC-E, and REC-F output lines. If the first half of IC 24 is activated, the selected incoming signal will be connected to the REC-G, REC-J, REC-K, and REC-L output lines. If the second half of IC 24 is activated, the selected incoming signal will be connected to the REC-M, REC-N, and REC-P output lines. Since IC 23 and IC 24 are inverters and the input buffers of each of the incoming signals are inverters, the resulting looped back signal is the same as the original incoming signal.

Looping Back the 4 Designated Clock Input Signals

Looping back the 4 input signals described in section 3.1.3 is accomplished by programming data positions B, and F.

When a "3" is programmed in the B position for loop back testing, a high is on IC 35 pin 5 and IC 36 pin 5. The high on IC 35 pin 5 is connected to IC 26 pin 19, and IC 19 through 22 pins 1 and 19. The drivers IC 19, IC 20, IC 21, IC 22, and half of IC 23 will be disabled and their output pins will be at a high impedance. The high on IC36 pin 5 is connected to IC 25 pin 4. Since IC 25 is an inverter, IC 25 pin 16 will be low. IC 25 pin 16 is connected to IC 25 pin 19 and IC 32 pin 1. The low on IC 25 pin 19 activates the drivers connected to output pins 9, 7, 5, and 3. The low on IC 32 pin 1 activates the first half of this decoder/demultiplexer. Since IC 32 pin 15 is connected to ground the second half of this IC is always activated.

Once the card has been set for loop back by programming data position B, CLK-1, CLK-2, CLK-3, or CLK-4 can be selected for loop back to DEL-CK by programming position F. The position F talk 2^0 and 2^1 data from IC 35 pin 10 and IC 36 pin 10 respectively is connected to the select input pins 11 and 10 of multiplexer IC 30. The multiplexer inputs of IC 30 are connected to the input CLK-1, CLK-2, CLK-3, and CLK-4 and are selected by the position F talk data present at pins 11 and 10. The inverted output of IC 30 is connected to St 4 pin 20 (DEL CK). If data position F is programmed to "0", input pin 4 of IC 30 (CLK-1) will be connected to the inverted output pin 6 (DEL CK). If data position F is programmed to "1", input pin 3 of IC 30 (CLK-2) will be connected to the inverted output pin 6 (DEL CK). If data position F is programmed to "2", input pin 2 of IC 30 (CLK-3) will be connected to the

inverted output pin 6 (DEL CK). If data position F is programmed to "3", input pin 1 of IC 30 (CLK-4) will be connected to the inverted output pin 6 (DEL CK). Since CLK-1, CLK-2, CLK-3, and CLK-4 are inverted by the buffers IC 6 and IC 25, and again by the multiplexer IC 30, the resulting looped back signal is the inverse of the original incoming signal.

3.3.4 Output Signals (Receive from UUT)

Each of these signal lines are terminated on the Digital Interface Module by 220Ω to +5 volts and 330Ω to ground. These termination networks are shown on the schematic as a "T".

Enabling and Disabling Motherboard Connections

The receive signals from the motherboard can be enabled or disabled by programming data position B. By programming the 2^0 bit to a 1 in the B data position, the signal path from the UTI-1 motherboard will be disabled; therefore any odd number programmed in this position will disable the motherboard connections. By programming the 2^0 bit to a 0 in the B data position, the signal path from the UTI-1 motherboard will be enabled; therefore, any even number or a "0" programmed in this position will enable the motherboard connections.

When a odd number is programmed in the B position, a high will be present at IC 35 pin 5. This pin is connected to IC 26 pin 19 and the $\overline{1G}$ and $\overline{2G}$ pins of IC 21 and IC 22. Half of IC 26 and all of IC 21 and IC 22 will be disabled and the appropriate output pins will be at a high impedance.

When a "0" or even number is programmed in the B position, a low will be present at IC 35 pin 5. Half of IC 26 and all of IC 21 and IC 22 will be enabled. Since IC 26, IC 21, and IC 22 are inverters, the data at St 4 will be the inverse of the original signals on St 1 and St 2.

Enabling and Disabling the Bu 1 (ITA) Connections

The receive signals from Bu1 can be enabled or disabled by programming data position B. By programming a "5" in the B data position, the signal path from Bu1 will be enabled. Since a "5" consists of a 2^0 (1) and a 2^2 (4) data bit, the 2^0 bit disables the signal path from the UTI-1 motherboard, and the 2^2 bit enables the signal path from Bu1. When the 2^2 (4) data bit is programmed is programmed to "0", the signal path from Bu1 will be disabled.

When a "1" or odd number is programmed in the B position, a high will be present at IC 35 pin 5. This pin is connected to IC 26 pin 19 and the $\overline{1G}$ and $\overline{2G}$ pins of IC 21 and IC 22. Half of IC 26 and all of IC 21 and IC 22 will be disabled and the appropriate output pins will be at a high impedance.

When a "1" is programmed in the B data position 2^2 bit, a high will be present at IC 37 pin 5. This pin is connected to IC 25 pin 6. The inverted output of this buffer pin 14 will be low. This low will enable one half of IC 26 and all of IC 19 and IC 20. Since IC 26, IC 19, and IC 20 are inverters, the data at St4 will be inverse of the original signals on Bu1.

When a "0" is programmed in the B data position 2^2 bit, a low will be present at IC 37 pin 5. This pin is connected to IC 25 pin 6. The inverted output of this buffer pin 14 will be high. This high will disable one half of IC 26 and all of IC 19 and IC 20. The outputs of one half of IC 26 and all of IC 19 and IC 20 will be at a high impedance.

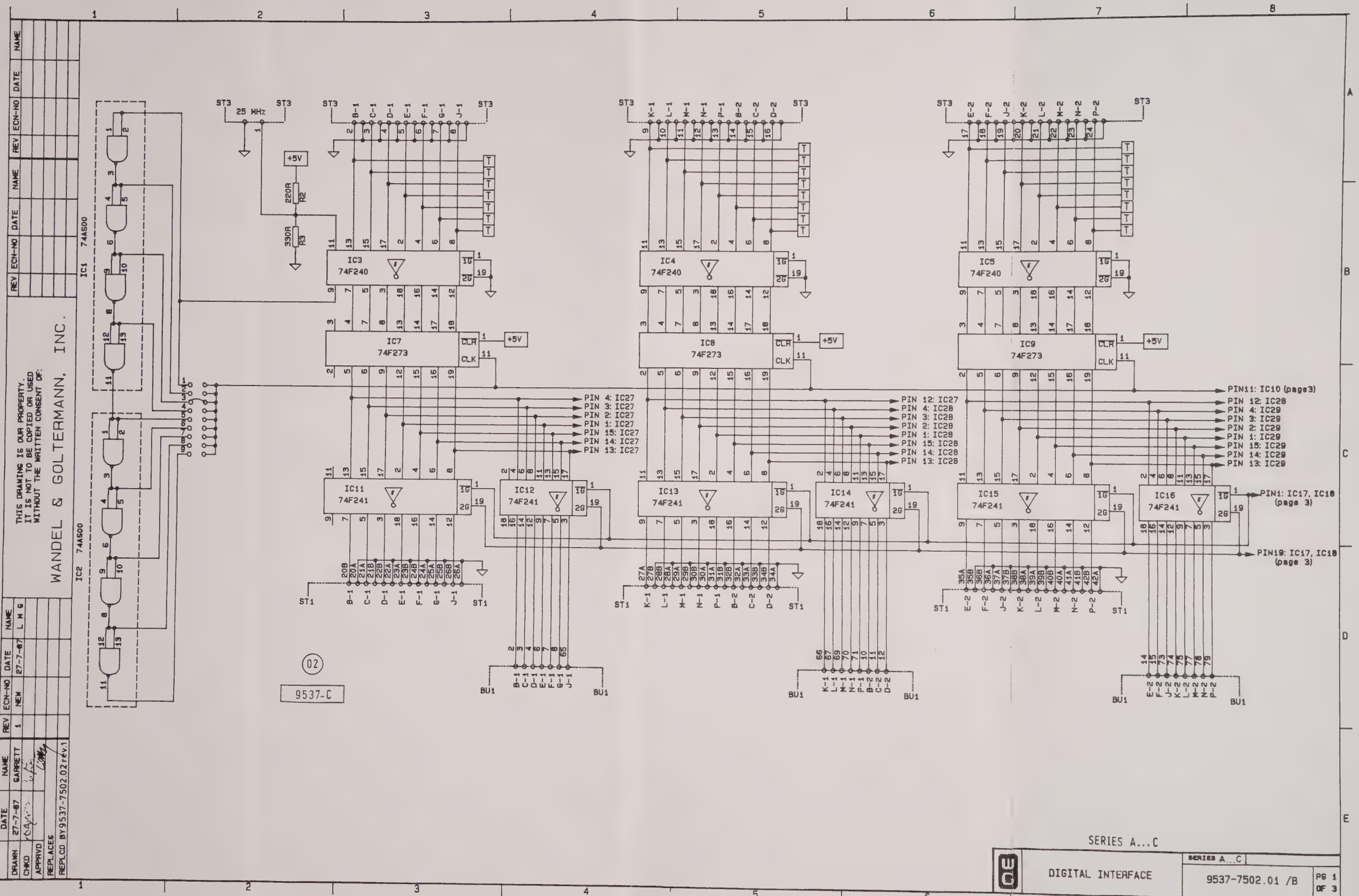
3.3.5 External Start Signal

After the card has been set to loop back by programming a "3" in data position B, the EXT STR line pin 21 of St 4 can be toggled between a low and a high. This is accomplished by programming a "1" or a "0" respectively in the G data position.

When a "3" is programmed in the B position for loop back testing, a high is on IC 35 pin 5 and IC 36 pin 5. The high on IC 35 pin 5 is connected to IC 26 pin 19, and IC 19 through 22 pins 1 and 19. The drivers IC 19, IC 20, IC 21, IC 22, and half of IC 23 will be disabled and their output pins will be at a high impedance. The high on IC36 pin 5 is connected to IC 25 pin 4. Since IC 25 is an inverter, IC 25 pin 16 will be low. IC 25 pin 16 is connected to IC 25 pin 19 and IC 32 pin 1. The low on IC 25 pin 19 activates the drivers connected to output pins 9, 7, 5, and 3. The low on IC 32 pin 1 activates the first half of this decoder/demultiplexer. Since IC 32 pin 15 is connected to ground the second half of this IC is always activated.

When a "0" is programmed in the G position, IC 35 pin 11 will be set low. This pin is connected to IC 25 pin 15. Since IC 25 is an inverter, the output pin 5 and St 4 pin 21 (EXT STR) will be set to high.

When a "1" is programmed in the G position, IC 35 pin 11 will be set high. This pin is connected to IC 25 pin 15. Since IC 25 is an inverter, the output pin 5 and St 4 pin 21 (EXT STR) will be set to low.



THIS DRAWING IS OUR PROPERTY. IT IS NOT TO BE COPIED OR USED WITHOUT THE WRITTEN CONSENT OF:

WANDEL & GOLTERMANN, INC.

REV	ECN-NO	DATE	NAME
1	NEW	27-7-87	L M G

	DATE	NAME
DRAWN	27-7-87	GARRETT
CHKD		
APPRVD		
REPLACES		
REPLCD BY	9537-7502.02 rev.1	

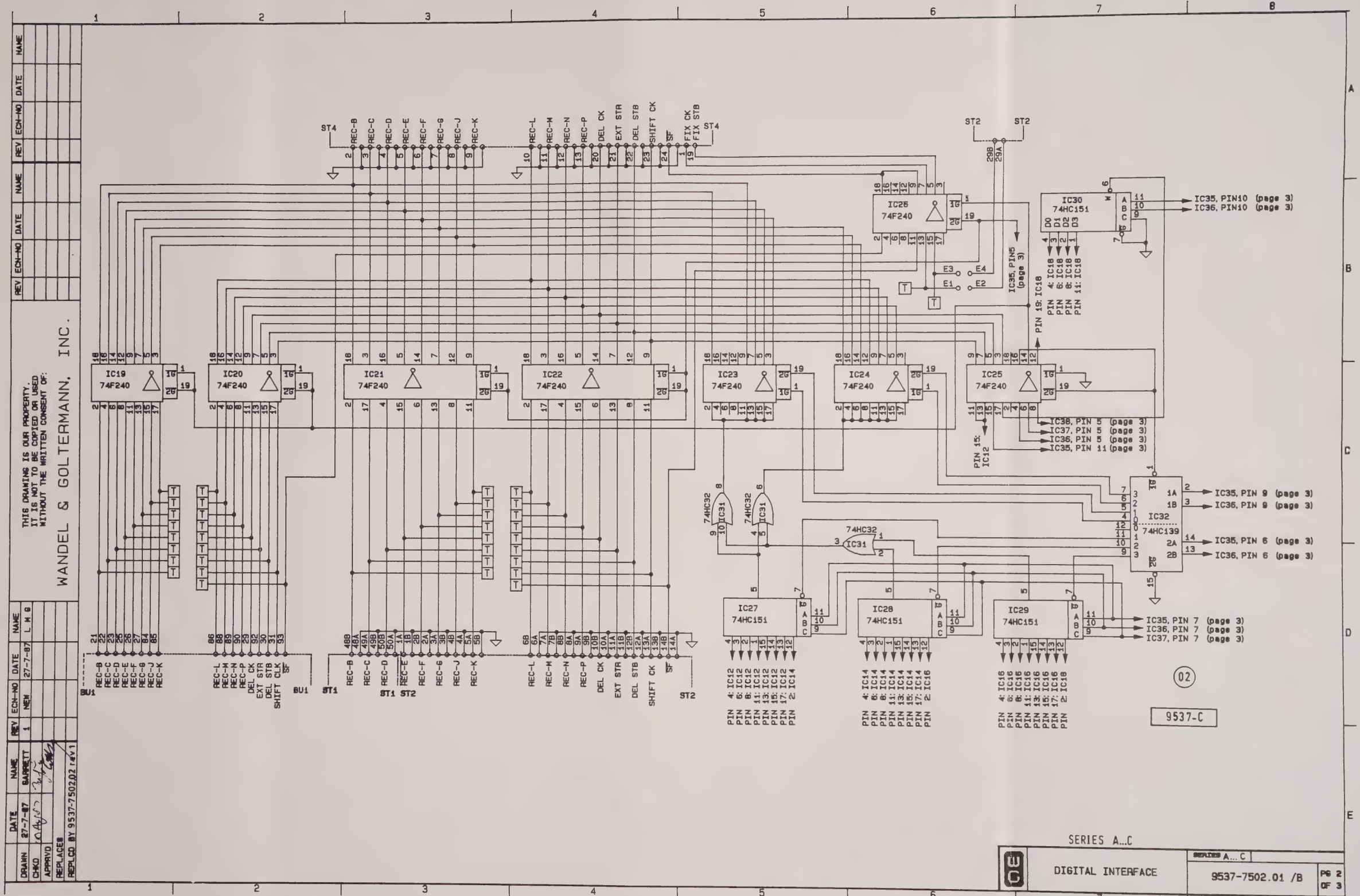
SERIES A...C

DIGITAL INTERFACE

SERIES A...C

9537-7502.01 /B

PG 1 OF 3



THIS DRAWING IS OUR PROPERTY.
IT IS NOT TO BE COPIED OR USED
WITHOUT THE WRITTEN CONSENT OF:
WANDEL & GOLTERMANN, INC.

REV	ECN-NO	DATE	NAME

	NAME	DATE
DRAWN	BARRETT	27-7-87
CHKD		
APPRVD		

REV	ECN-NO	DATE	NAME
1	NEW	27-7-87	L M G

REPLACES
REPLCD BY 9537-7502.02 rev1

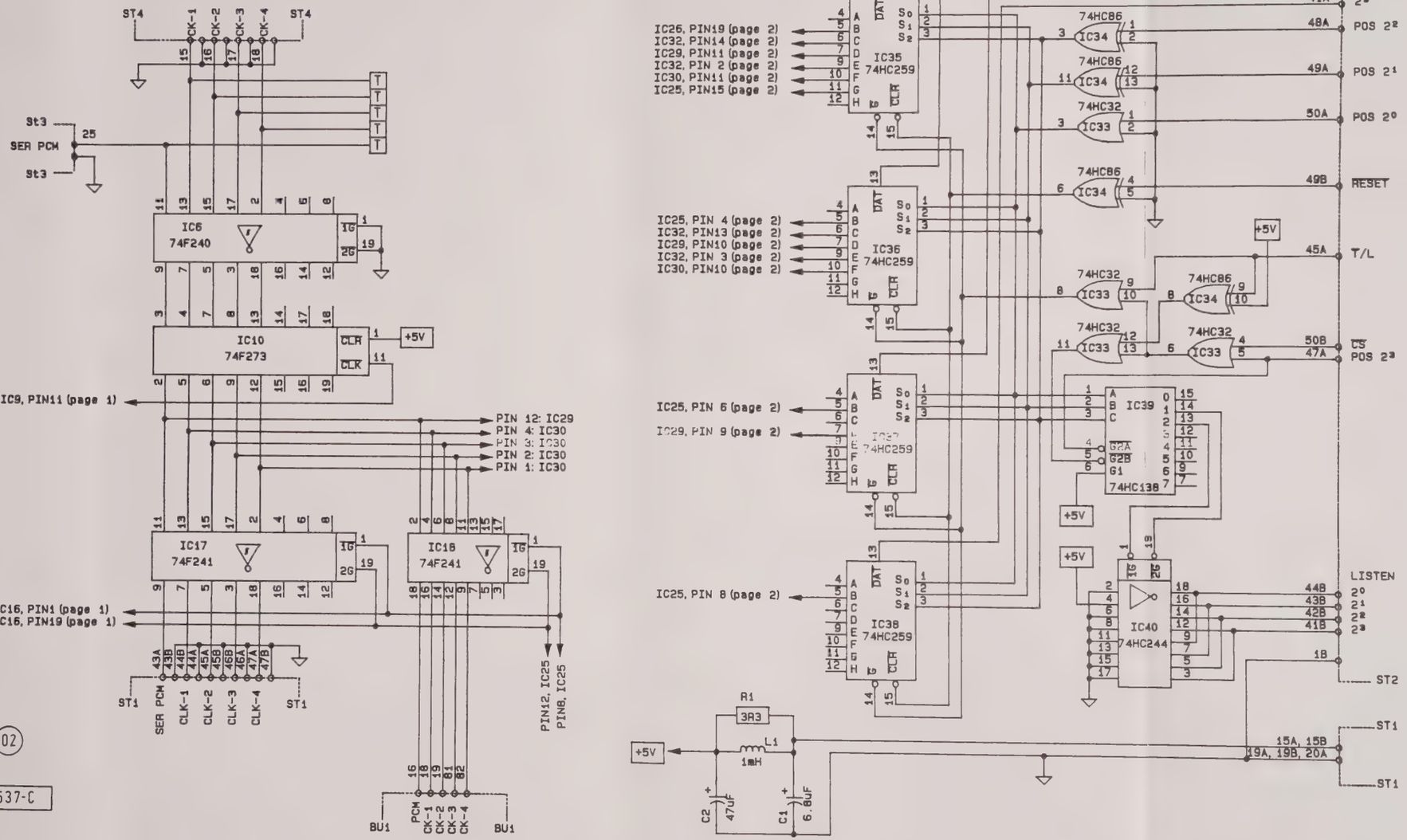
SERIES A...C

DIGITAL INTERFACE

SERIES A... C

9537-7502.01 /B

PG 2 OF 3



02

9537-C

THIS DRAWING IS OUR PROPERTY.
IT IS NOT TO BE COPIED OR USED
WITHOUT THE WRITTEN CONSENT OF:

WANDEL & GOLTERMANN, INC.

	REV	ECN-NO	DATE	NAME
	1	NEW	30-7-87	L M G

	DATE	NAME
DRAWN	27-7-87	GARRETT
CHKD		
APPRVD		

REPLACES

REPLCD BY 9537-7502.04rev1

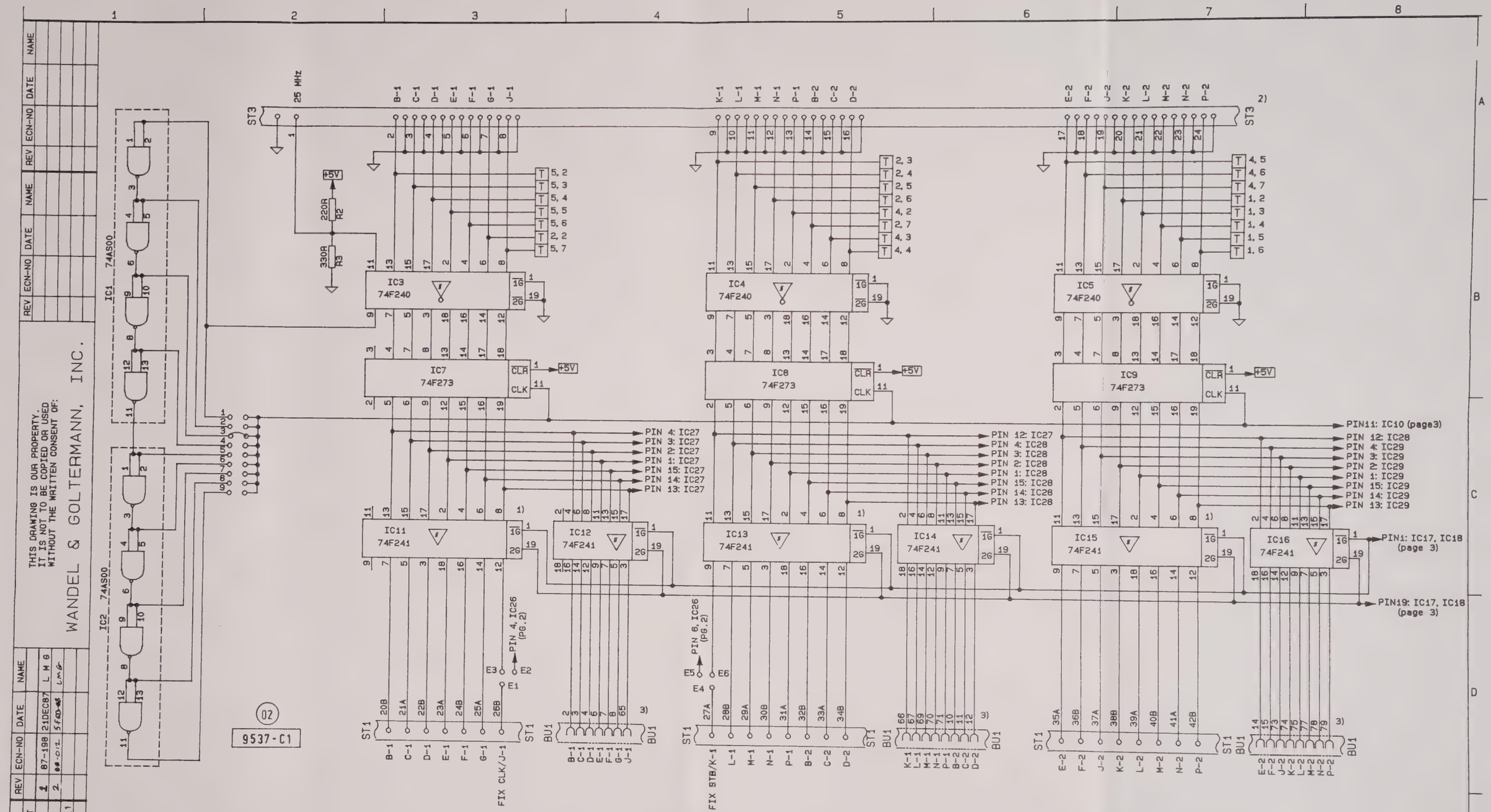
SERIES A...C

DIGITAL INTERFACE

SERIES A...C

9537-7502.01 /B

PG 3 OF 3



NOTES:
1) THESE COMPONENTS ARE NOT INSTALLED DURING ASSEMBLY. THEY MAY BE INSTALLED OPTIONALLY AT A LATER TIME.
2) ST3, ST4 PINS 26 THRU 50 ARE GROUND.
3) BU1 PINS 1, 5, 9, 13, 17, 20, 28, 33 THROUGH 63, 64, 72, 76, 80, 83, 87, 91, 95 ARE GROUND.

THIS DRAWING IS OUR PROPERTY. IT IS NOT TO BE COPIED OR USED WITHOUT THE WRITTEN CONSENT OF:
WANDEL & GOLTERMANN, INC.

REV	ECN-NO	DATE	NAME
1	87-198	21DEC87	L M G
2	88-012	5FEB88	LMG

	DATE	NAME
DRAWN	27-7-87	GARRETT
CHKD	6 Jan 87	
APPRVD		
REPLACES 9537-7502.01 REV.1		
REPLCD BY		

DIGITAL INTERFACE

SERIES D...

9537-7502.~~01~~ 02 /B

PG 1 OF 3

THIS DRAWING IS OUR PROPERTY. IT IS NOT TO BE COPIED OR USED WITHOUT THE WRITTEN CONSENT OF:

WANDEL & GOLTERMANN, INC.

	NAME	DATE	ECN-NO	REV	NAME	DATE	ECN-NO	REV
DRAWN	GARRETT	27-7-87						
CHKD		18-1-88	87-198	1	L M G	21DEC87		
APPRVD			88-015	2	L M G	5 FEB 88		

REPLACES 9537-7502.01 REV 1

REPLCD BY

NOTES:
1) THESE COMPONENTS ARE NOT INSTALLED DURING ASSEMBLY. THEY MAY BE INSTALLED OPTIONALLY AT A LATER TIME.
2) ST3, ST4 PINS 26 THRU 50 ARE GROUND.
3) BU1 PINS 1, 5, 9, 13, 17, 20, 28, 33 THROUGH 63, 64, 72, 76, 80, 83, 87, 91, 95 ARE GROUND.

DIGITAL INTERFACE

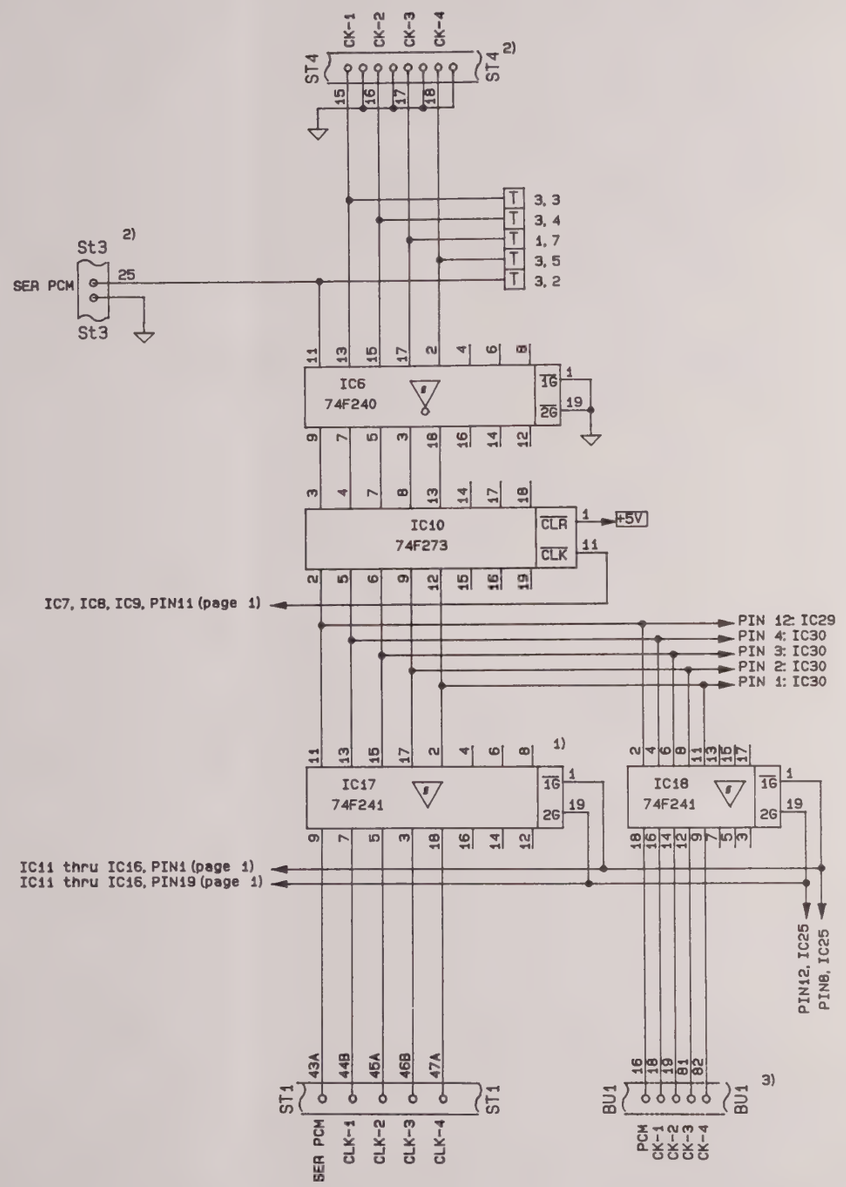
SERIES D...

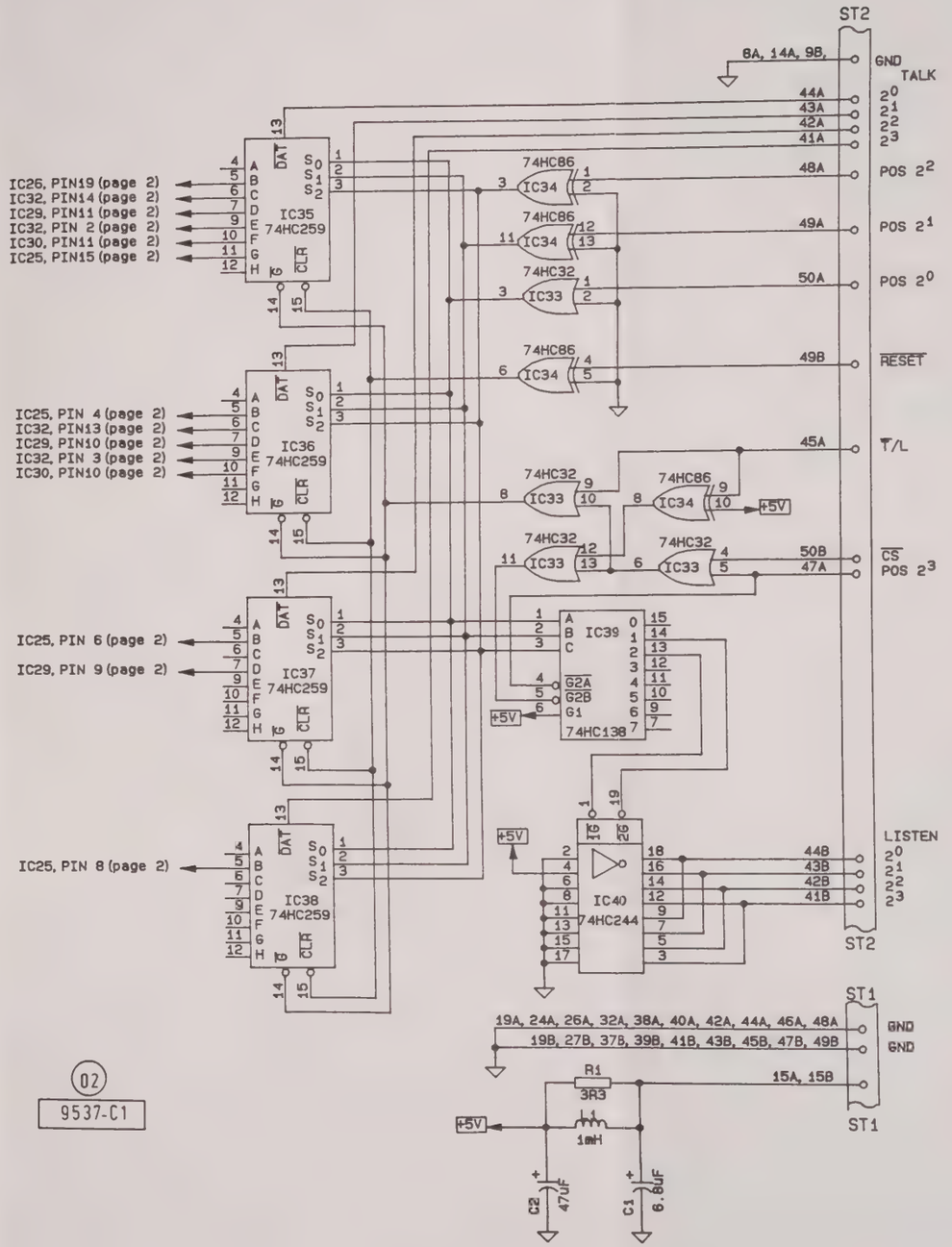
9537-7502.02 /B

PG 2 OF 3

02

9537-C1





02
9537-C1

NOTES:
1) THESE COMPONENTS ARE NOT INSTALLED DURING ASSEMBLY. THEY MAY BE INSTALLED OPTIONALLY AT A LATER TIME.
2) ST3, ST4 PINS 26 THRU 50 ARE GROUND.
3) BU1 PINS 1, 5, 9, 13, 17, 20, 28, 33 THROUGH 63, 64, 72, 76, 80, 83, 87, 91, 95 ARE GROUND.

REV	ECN-NO	DATE	NAME
1	87-198	21DEC87	L.M.G
2	88-012	5FEB88	L.M.G

	NAME	DATE
DRAWN	GARRETT	27-7-87
CHKD		
APPRVD		

REPLACES 9537.7502.01 /REV.1
REPLCD BY

THIS DRAWING IS OUR PROPERTY.
IT IS NOT TO BE COPIED OR USED
WITHOUT THE WRITTEN CONSENT OF:
WANDEL & GOLTERMANN, INC.

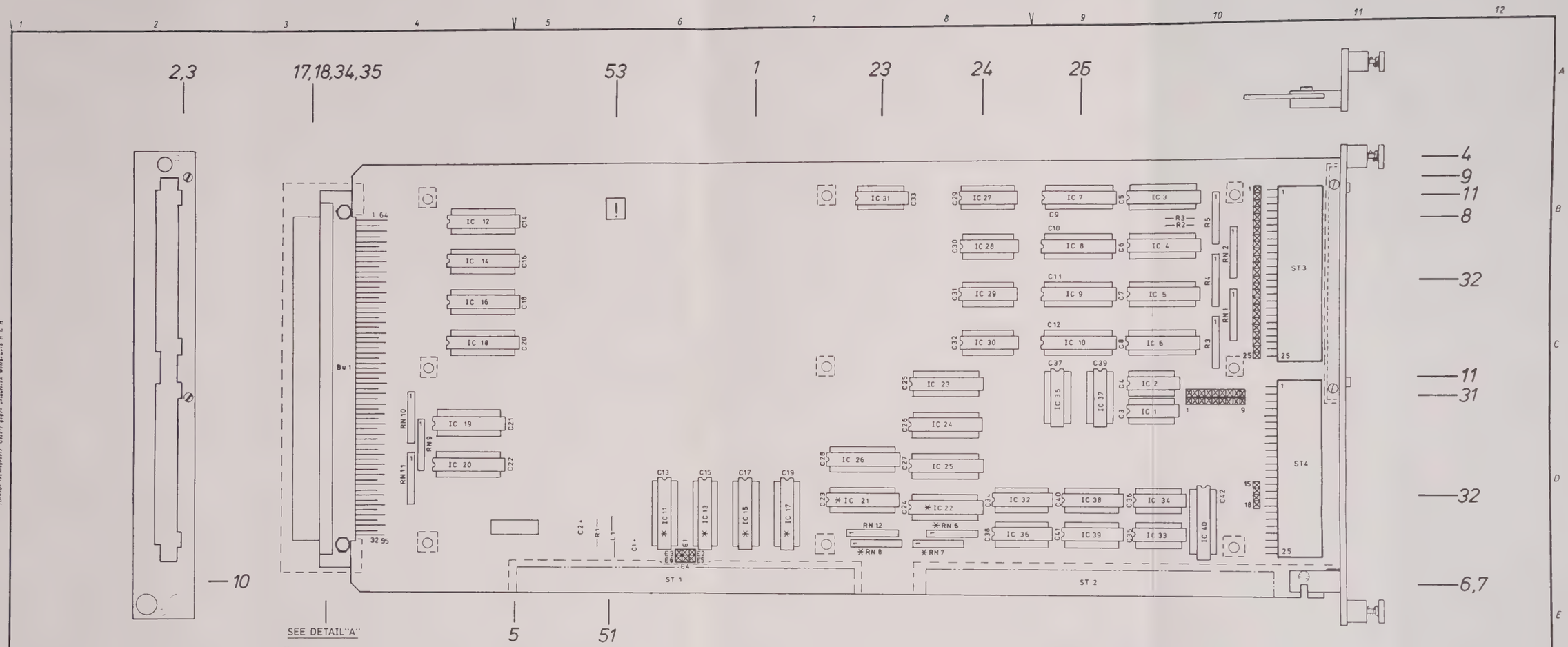
GE

DIGITAL INTERFACE

SERIES D...

9537-7502.~~01~~ 02 /B

PG 3 OF 3



DETAIL "A"

PINS 33 TO 63 ARE FOR FUTURE USE AND ARE NOT AVAILABLE IN THIS SERIES ACTUAL BU1 CONN IS MARKED PINS 1 THRU 64 DETAIL DWG SHOWS PROPER PIN #'S AND LOCATION.

□ Soldermask these areas using items 50 & 52.

* Items RN6,7,8,ICs11,13,15,17,21,22 and their respective sockets are optional. Their PC board locations are to be soldermask when they are not included on partslist.

Oberfläche FOR SERIES D

Aus-gabe	Änderung	Tag	Name
7	88-059	13.4.88	LMG
6	87-198	12.17.87	RHS
5	ECN 87-163	18-11-87	DHB
4	ECN 87-138	10-8-87	
3	ECN 87-093	27.7.87	LG
2	87-066	4.6.87	LGG
1	New	8.3.87	LGG

Freimaßtoleranzen: WN 51/3/1

	Tag	Name
Bearb	18.3.87	Lex Garrett
Gepr.	26.3.87	Sanjay D.
Norm.		WTM

Wandel u. Goltermann Reutlingen

Halbzeug und Werkstoffe

Benennung: INTERFACE, DIGITAL (ASSEMBLED) 9537-C1

Maßstab: 1/1

9537-7002.00 /34

REPLACES: 9537-7002.00 rev.5

Erstm. Verwdg

WANDEL & GOLTERMANN TECHNOLOGIES, INC.
DIGITAL SIGNAL INTERFACE MODULE

BN 9537 ********** LIST OF REPLACEABLE PARTS ********** SERIES: ALL
DATE: Jan 8, 1990

DIAG	REF	ITEM	QTY	PART NUMBER	DESCRIPTION	STOCK LOCATION	VERS/OPT	SERIES STRT	SERIES END	SUBASSEMBLY 9537-XXXX	SUBASSEMBLY CODE
							00 02			7002	S
		0	0	9537-7002.005	DIGITAL INTERFACE		00 02			7002	A
		1	1	9537-7002.021	PC BOARD MACHINED		00 02			7002	
		3	1	9537-7002.050	PANEL REAR MARKED		00 02			7002	
		5	1	0000-2911.029	LABEL SERIAL ABC		00 02			7002	
		6	1	9537-7001.064	BLOCK PANEL MTG 1		00 02			7002	
		8	1	9537-7002.063	BAR PNL SUPPORT 84mm		00 02			7002	
		13	0	9537-7001.077	SHIELD PCB EMI/RFI		00 02			7002	
		31	0		HEADR STR AU M1X36P	XX03-0375.00	00 02			7002	M
		32	0		HEADR STR AU M1X36P	XX03-0375.00	00 02			7002	M
		33	0		HEADR STR AU M1X36P	XX03-0375.00	00 02			7002	M
		34	0		HEADR STR AU M1X36P	XX03-0375.00	00 02			7002	M
		34	32		RECEPT PIN ANG ROW#1	XX03-0517.00	00 02	D		7002	
		35	32		RECEPT PIN ANG ROW#3	XX03-0518.00	00 02	D		7002	
		51	.1		TUBNG SHRNK 1/4" BLK	XX31 0005.00	00 02			7002	
		53	1	0001-0072.468	LABEL YEL/BLK C-MOS		00 02			7002	
02	BU	1	1		CONN ANG PC MT F64P	XX03-0521.00	00 02		C	7002	
02	BU	1	1	9537-0000.101	CONN MODIFIED 64P		00 02	D		7002	M
02	C	1	1		C-ELYT TA 6.8U10%35V	XX32-0006.00	00 02			7002	
02	C	2	1		C-ELYT TA 47u 10%20V	XX32-0096.00	00 02			7002	
02	C	3	1	0000-7632.659	C CER 100N 10% 50V		00 02			7002	
02	C	4	1	0000-7632.659	C-CER 100N 10% 50V		00 02			7002	
02	C	5	1	0000-7632.659	C CER 100N 10% 50V		00 02			7002	
02	C	6	1	0000-7632.659	C-CER 100N 10% 50V		00 02			7002	
02	C	7	1	0000-7632.659	C-CER 100N 10% 50V		00 02			7002	
02	C	8	1	0000-7632.659	C-CER 100N 10% 50V		00 02			7002	
02	C	9	1	0000-7632.659	C-CER 100N 10% 50V		00 02			7002	
02	C	10	1	0000-7632.659	C-CER 100N 10% 50V		00 02			7002	
02	C	11	1	0000-7632.659	C-CER 100N 10% 50V		00 02			7002	
02	C	12	1	0000-7632.659	C-CER 100N 10% 50V		00 02			7002	
02	C	13	1	0000-7632.659	C CER 100N 10% 50V		00 02			7002	
02	C	14	1	0000-7632.659	C-CER 100N 10% 50V		00 02			7002	
02	C	15	1	0000-7632.659	C-CER 100N 10% 50V		00 02			7002	
02	C	16	1	0000-7632.659	C-CER 100N 10% 50V		00 02			7002	
02	C	17	1	0000-7632.659	C CER 100N 10% 50V		00 02			7002	
02	C	18	1	0000-7632.659	C CER 100N 10% 50V		00 02			7002	

WANDEL & GOLTERMANN TECHNOLOGIES, INC.

DIGITAL SIGNAL INTERFACE MODULE

BN 9537 ********** LIST OF REPLACEABLE PARTS ********** SERIES: ALL DATE: Jan 8, 1990

DIAG	REF	ITEM	QTY	PART NUMBER	DESCRIPTION		STOCK LOCATION	VERS/OPT	SERIES STRT	SERIES END	SUBASSEMBLY 9537-XXXX CODE
02	C	19	1	0000-7632.659	C-CER 100N 10%	50V		00 02			7002
02	C	20	1	0000-7632.659	C-CER 100N 10%	50V		00 02			7002
02	C	21	1	0000-7632.659	C-CER 100N 10%	50V		00 02			7002
02	C	22	1	0000-7632.659	C-CER 100N 10%	50V		00 02			7002
02	C	23	1	0000-7632.659	C-CER 100N 10%	50V		00 02			7002
02	C	24	1	0000-7632.659	C-CER 100N 10%	50V		00 02			7002
02	C	25	1	0000-7632.659	C-CER 100N 10%	50V		00 02			7002
02	C	26	1	0000-7632.659	C-CER 100N 10%	50V		00 02			7002
02	C	27	1	0000-7632.659	C-CER 100N 10%	50V		00 02			7002
02	C	28	1	0000-7632.659	C-CER 100N 10%	50V		00 02			7002
02	C	29	1	0000-7632.659	C-CER 100N 10%	50V		00 02			7002
02	C	30	1	0000-7632.659	C-CER 100N 10%	50V		00 02			7002
02	C	31	1	0000-7632.659	C-CER 100N 10%	50V		00 02			7002
02	C	32	1	0000-7632.659	C-CER 100N 10%	50V		00 02			7002
02	C	33	1	0000-7632.659	C-CER 100N 10%	50V		00 02			7002
02	C	34	1	0000-7632.659	C-CER 100N 10%	50V		00 02			7002
02	C	35	1	0000-7632.659	C-CER 100N 10%	50V		00 02			7002
02	C	36	1	0000-7632.659	C-CER 100N 10%	50V		00 02			7002
02	C	37	1	0000-7632.659	C-CER 100N 10%	50V		00 02			7002
02	C	38	1	0000-7632.659	C-CER 100N 10%	50V		00 02			7002
02	C	39	1	0000-7632.659	C-CER 100N 10%	50V		00 02			7002
02	C	40	1	0000-7632.659	C-CER 100N 10%	50V		00 02			7002
02	C	41	1	0000-7632.659	C-CER 100N 10%	50V		00 02			7002
02	C	42	1	0000-7632.659	C-CER 100N 10%	50V		00 02			7002
02	IC	1	1	0001-0066.432	IC TTL 74LS00	D14		00 02			7002
02	IC	2	1	0001-0066.432	IC TTL 74LS00	D14		00 02			7002
02	IC	3	1		IC TTL 74F240		XX35-0507.00	00 02			7002
02	IC	4	1		IC TTL 74F240		XX35-0507.00	00 02			7002
02	IC	5	1		IC TTL 74F240		XX35-0507.00	00 02			7002
02	IC	6	1		IC TTL 74F240		XX35-0507.00	00 02			7002
02	IC	7	1	0000-7672.376	IC TTL 74F273	D20		00 02			7002
02	IC	8	1	0000-7672.376	IC TTL 74F273	D20		00 02			7002
02	IC	9	1	0000-7672.376	IC TTL 74F273	D20		00 02			7002
02	IC	10	1	0000-7672.376	IC TTL 74F273	D20		00 02			7002
00	IC	11	0		IC TTL 74F241		XX35-0506.00	00 02			7002
02	IC	12	1		IC TTL 74F241		XX35-0506.00	00 02			7002

WANDEL & GOLTERMANN TECHNOLOGIES, INC.
DIGITAL SIGNAL INTERFACE MODULE

BN 9537 ********** LIST OF REPLACEABLE PARTS ********** SERIES: ALL
DATE: Jan 8, 1990

DIAG	REF	ITEM	QTY	PART NUMBER	DESCRIPTION	STOCK LOCATION	VERS/OPT	SERIES STRT	SERIES END	SUBASSEMBLY 9537-XXXX CODE
02	RN	5	1		R-PACK 6X221/331 OHM	XX08-0696.00	00 02			7002
02	RN	6	0		R-PACK 6X221/331 OHM	XX08-0696.00	00 02			7002
02	RN	7	0		R-PACK 6X221/331 OHM	XX08-0696.00	00 02			7002
02	RN	8	0		R-PACK 6X221/331 OHM	XX08-0696.00	00 02			7002
02	RN	9	1		R-PACK 6X221/331 OHM	XX08-0696.00	00 02			7002
02	RN	10	1		R-PACK 6X221/331 OHM	XX08-0696.00	00 02			7002
02	RN	11	1		R-PACK 6X221/331 OHM	XX08-0696.00	00 02			7002
02	RN	12	1		R-PACK 6X221/331 OHM	XX08-0696.00	00 02			7002
02	ST	2	1		CONN HEADR ANG 2X25M	XX03-0503.00	00 02			7002
02	ST	3	1		CONN HEADR ANG 2X25M	XX03-0503.00	00 02			7002

Analog Interface Module BN 9537/00.03

Contents

		Page
1.	Introduction	.1-1
2.	Specifications	.2-1
2.1.	DC Characteristics	.2-1
2.2.	Analog Balanced Busses	.2-1
2.3.	Coaxial Monitor Busses	.2-2
2.4.	Balanced / Single Ended Converstion	.2-2
2.4.1	Balanced to Single Ended Amplifier	.2-2
2.4.2	Single Ended to Balanced Amplifier	.2-3
2.5.	Supply Voltages	.2-3
2.5.1	General Supply Voltages	.2-3
2.5.2	Auxiliary Voltages	.2-3
2.6.	Relay Ratings	.2-3
3.	Operating Description	.3-1
3.1.	Detailed Description of Features	.3-1
3.1.1	General Supply Voltage Connections	.3-1
3.1.2	Auxiliary Supply Voltage Connections	.3-2
3.1.3	Transmit and Receive Signal Connections	.3-3
3.1.4	Other Analog Buses	.3-4
3.1.5	Digital Multimeter Bus	.3-5
3.1.6	Coaxial Connections	.3-5
3.1.7	Signal Flow Chart and Pin Connections	.3-7
3.2.	Programming	3-13
3.2.1	Programming Sheets	3-13
3.2.2	Programming Description	3-19
3.2.2.1	Programming Position A	3-19
3.2.2.2	Programming Position B	3-19
3.2.2.3	Programming Position C	3-19
3.2.2.4	Programming Positions D and E	3-19
3.2.2.5	Programming Positions F and G	3-19
3.2.2.6	Programming Position H	3-19
3.2.2.7	Reading the Card ID	3-20
3.2.3	Programming Example	3-20
3.3.	Circuit Description	3-21
3.3.1	4 Bit Parallel Bus	3-21
3.3.2	Digital Multimeter Interface	3-21
3.3.3	General Power Supply Interface	3-22
3.3.4	Auxiliary Power Supply Interface	3-22
3.3.5	Analog Bus 2	3-23
3.3.6	Analog Bus 3	3-24
3.3.7	Spare Analog Busses	3-24
3.3.8	Coaxial Monitor Busses	3-24
3.4.	Schematic Diagram / Parts List	3-25

Analog Interface Module Description and Operation

1. Introduction

The Analog Interface Module interconnects analog test signals between the test system and the UUT. Six balanced analog busses can be connected through connectors provided on the rear panel. The first three busses are designed to handle DMM, transmit, and receive. The other three busses are identical and can be used to interface any analog signal desired. All balanced busses are available on the motherboard as well as on the front connector.

2. Specifications

2.1. DC Characteristics

Maximum power consumption per module

1) Power consumption during normal usage. DMM (Bu 5), Tx (Bu 6), Rx (Bu 7), Spare (Bu 8), Spare (Bu 9) and Spare (Bu 10) are connected to the Motherboard or Interchangeable Test Adapter. The Tx and Rx ports are set to the single ended mode. V1 through V4 and all Auxiliary Supply Voltages are connected to the Motherboard or Interchangeable Test Adapter. The AC and DC Auxiliary Supply Voltages are combined.

	+5 V	+15 V	-15 V	Total
Current (Amps)	1.1	0.013	0.013	-----
Power (Watts)	6.5	0.2	0.2	6.50

2) Power consumption during minimal usage. DMM (Bu 5), Tx (Bu 6), and Rx (Bu 7) are connected to the Motherboard or Interchangeable Test Adapter. The Tx and Rx ports are set to the balanced mode. V1 through V4 and all Auxiliary Supply Voltages are connected to the Motheboard or Interchangeable Test Adapter. The AC and DC Auxiliary Supply Voltages are combined.

	+5 V	+15 V	-15 V	Total
Current (Amps)	0.6	0.013	0.013	-----
Power (Watts)	3.0	0.2	0.2	5.90

3) Power consumption with all relays energized. This condition is not typical.

	+5 V	+15 V	-15 V	Total
Current (Amps)	3.5	0.013	0.013	-----
Power (Watts)	17.5	0.2	0.2	17.90

2.2. Analog Balanced Busses

Number of Balanced Busses 6
Frequency Range . . . . . DC to 620 kHz
Relay Ratings . . . . . 1A @ 150V, 2A @ 30V

Rear Panel Connections to Bu1 Interchangeable Test Adapter Connections

Insertion Loss @ 1 kHz . . . . . ≤0.03 dB*
Frequency Response (referenced to 1 kHz)
DC to 10 kHz . . . . . ±0.03 dB*
10 kHz to 620 kHz . . . . . ±0.40 dB*
Crosstalk Attenuation between Busses
50 Hz to 10 kHz . . . . . <95 dB*
10 kHz to 620 kHz . . . . . <60 dB*

Rear Panel Connections to Motherboard Connections

Insertion Loss @ 1 kHz . . . . . ≤0.05 dB*
Frequency Response (referenced to 1 kHz)
DC to 10 kHz . . . . . ±0.05 dB*
10 kHz to 620 kHz . . . . . ±0.40 dB*
Crosstalk Attenuation between Busses
50 Hz to 10 kHz . . . . . <90 dB*
10 kHz to 620 kHz . . . . . <55 dB*
*Measurements at 600Ω termination

2.3. Coaxial Monitor Busses

Number of Connections 2
Frequency Range . . . . . DC to 620 kHz
Impedance . . . . . 50Ω or 75Ω
Insertion Loss @ 1 kHz . . . . . <0.03 dB*
Frequency Response (Referenced to 1 kHz)
DC to 620 kHz . . . . . <10 dB*
Crosstalk Attenuation between Busses
Frequency <10 kHz . . . . . <90 dB*
10 kHz to 620 kHz . . . . . <65 dB*
*Measurements at 75Ω termination

2.4. Balanced / Single-ended Conversion

2.4.1 Balanced to Single-ended Conversion (Transmit Path)

Input/Output Impedance 600Ω
Gain . . . . . 6 dB 0.02 dB*
Frequency Range . . . . . 50 Hz to 620 kHz
Input Level Range . . . . . +10 to -60 dBm
Frequency Response (Referenced to 1 kHz)
50 Hz to 10 kHz . . . . . ±0.50 dB*
10 kHz to 620 kHz . . . . . ±0.50 dB*
Variation of Gain with Level @ 1 kHz
(referenced to -10 dBm)
Level Range: +10 to 0 dBm . . . . . ±0.02 dB*
Level Range: 0 to -40 dBm . . . . . ±0.05 dB*
Harmonic Ratio: Z in = Z out = 600Ω.
ak2, ak3 . . . . . ≥60 dB
Level Range: -40 to -60 dBm . . . . . ±0.10 dB
* Measurements at 600Ω termination

2.4.2 Single-ended to Balanced Amplifier

Output/Input Impedance 600Ω
Gain . . . . . 0 dB
Frequency Range . . . . . 50 Hz to 10 kHz
Input Level Range . . . . . +10 to -60 dBm
Absolute Level Accuracy . . . . . ±0.02 dB*
Frequency Response
    50 Hz to 10 kHz, Referenced to 1 kHz . . . . . ±0.10 dB*
Variation of Gain with Level @ 1 kHz
    (referenced to -10 dBM)
    Level Range: +10 to 0 dBm . . . . . ±0.02 dB*
    Level Range: 0 to -40 dBm . . . . . ±0.05 dB*
    Level Range: -40 to -60 dBm . . . . . ±0.10 dB*
Harmonic Ratio: Z in = Z out = 600Ω.
    ak2, ak3 . . . . . ≥60 dB
*Measurements at 600Ω termination

2.5. Supply Voltages

2.5.1 General Supply Voltages

Number of Voltage Lines 8
Maximum Power Load . . . . . 400 mA @ 150V, 4 A @ 15V

2.5.2 Auxiliary Voltages

Number of Voltage Lines 5
Maximum Power Load . . . . . 800 mA @ 150V, 8A @ 15V

2.6. Relay Ratings

Maximum Current . . . . . 1A @ 150V, 2A @ 30V

3. Operating Description

3.1. Detailed Description of Features

3.1.1 General Supply Voltage Connections

The voltage and sense lines from eight power supplies, V1 to V8, may be connected to the Analog Module at Bu3 and Bu4 on the rear panel. Each of these voltages can be switched individually to the ITA and the UTI-1 motherboard. All of these supplies are totally isolated from each other and from other circuitry; this means that the ground reference can be chosen at the Personality Module for each supply.

Each of these voltage supply lines can be monitored by a digital multimeter at the DMM port Bu5 on the rear panel. The DMM port will be described in further detail in section 3.1.5.

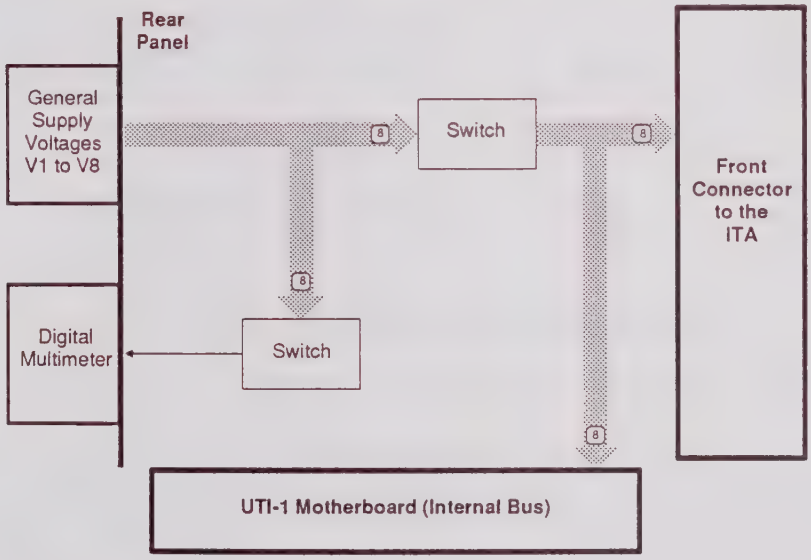


Figure 3.1.1 General Supply Voltage Connections

3.1.2 Auxiliary Supply Connections

The rear panel connection Bu2 is used for connecting auxiliary voltages. There is capacity for connecting three fixed voltages (AV 1, AV 2, and AV 3) of up to 150 volts. In addition, there is a pair of lines useful for programmable high DC voltage, AV 5, and another pair of lines for a programmable high AC voltage, AV 4.

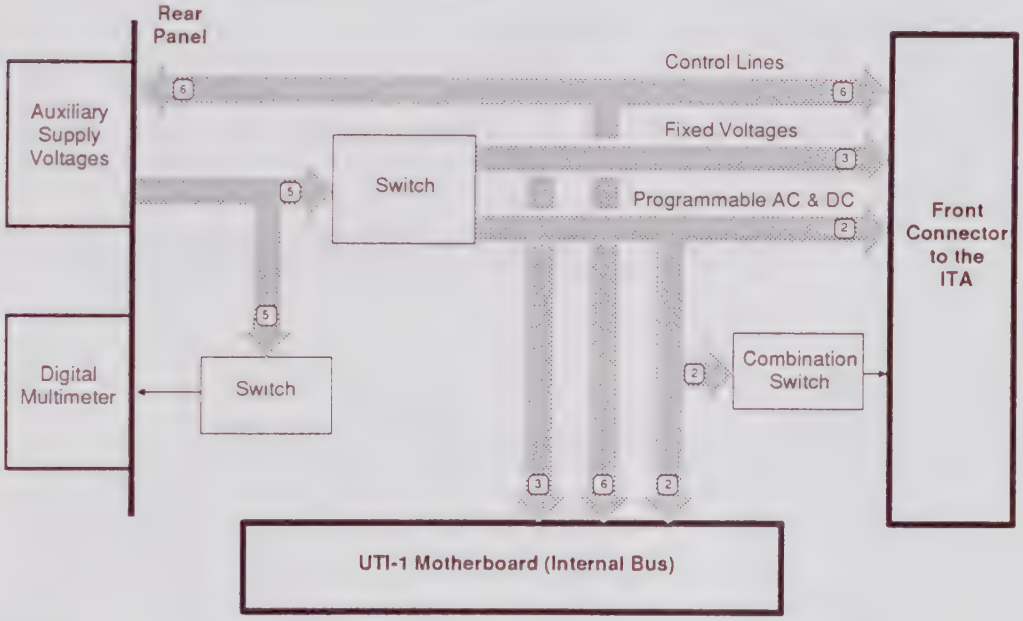


Figure 3.1.2 Auxiliary Supply Voltage Connections

AV 1 and AV 2 share a common reference line. See the schematic diagram for further details.

Circuitry on the Analog Module can combine the AV 4 and AV 5 voltages. Assuming that the two lines of AV 4 are both phases of an AC voltage and the two lines of AV 5 are the plus and minus outputs of a DC voltage, the combination of these two voltages at the AV 4/5 output pins is as follows:

1. AC and -DC separate: One side of the AC and the +DC are grounded. The AC goes to the L pin, and the -DC goes to the H pin.
2. AC superimposed on -DC: The AC signal is superimposed on the -DC signal and located at the H pin. The L pin is grounded.
3. AC and +DC separate: One side of the AC and the -DC are grounded. The AC goes to the L pin, and the +DC goes to the H pin.
4. AC superimposed on +DC: The AC signal is superimposed on the +DC signal and located at the H pin. The L pin is grounded.
5. H and L swapped: This function can be used with any of the above combinations, and causes the signals on the H and L pins to be reversed.

There are six additional lines from Bu2 which may be used as control lines in conjunction with these auxiliary voltages.

Each of the auxiliary supply voltage lines can be monitored by a digital multimeter at the DMM port Bu5 on the rear panel. The DMM port will be described in further detail in section 3.1.5.

3.1.3 Transmit and Receive Signal Connections

Of the six balanced analog busses, two are normally used for the transmit and receive signals. Bus AB2 (located at Bu6 rear panel connection) is used for the transmit signals and bus AB3 (located at Bu7 rear panel connection) is used for the receive signal.

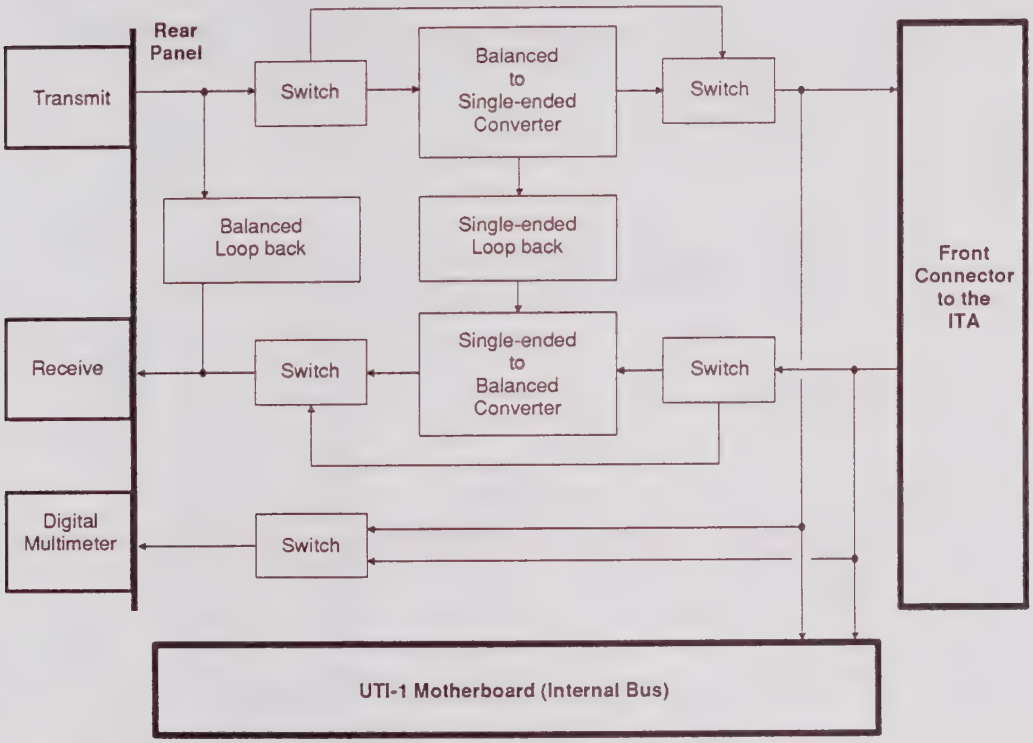


Figure 3.1.3 Transmit and Receive Bus Connections

The transmit signal may be used as is or may be converted to low impedance and single-ended by an on-board balanced to single-ended amplifier. The amplifier expects its input to come from a 600Ω external source, and it increases the level of this signal by 6 dB. The analog transmit signal may be looped back to a external receiver via the analog receive port AB 3.

If the receive signal is balanced, it may be used as is. If the Personality Board or another UTI-1 returns a low impedance, single-ended signal, a single-ended to balanced amplifier on the Analog Module may be selected to convert the signal to 600Ω balanced without a change in level.

The analog transmit signal may be looped back to an external receiver via the analog receive port AB 3. The loop back may be done balanced or single-ended. Loop back is made available for such purposes as calibrating the signal path or checking the test setup.

Both the transmit and receive lines can be monitored by a digital multimeter at the DMM port Bu5 on the rear panel. The DMM port will be described in further detail in section 3.1.5.

3.1.4 Other Analog Busses

AB 4, AB 5, and AB 6 are balanced analog busses and are connected to the rear panel connections Bu8, Bu9, and Bu10 respectively. These are straight connections to the UTI-1 motherboard's internal bus and the front connector for the Interchangeable Test Adapter (ITA).

Each of these busses can be monitored by a digital multimeter at the DMM port Bu5 on the rear panel. The DMM port will be described in further detail in section 3.1.5.

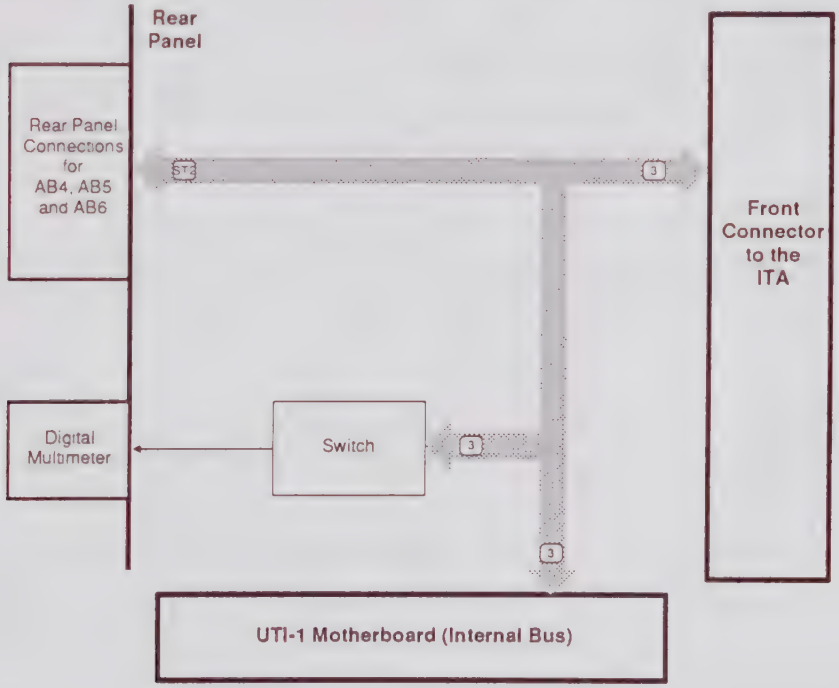


Figure 3.1.4 Additional Balanced Bus Connections

3.1.5 Digital Multimeter Bus

A digital multimeter or some other device may be connected to any of the voltages or signals mentioned above by the internal DMM bus on the Analog Module. The Analog Module will alternately connect this bus to the personality board or to any other module in the UTI-1 through the motherboard. Connection to this bus (AB 1) is made via the rear connector Bu5.

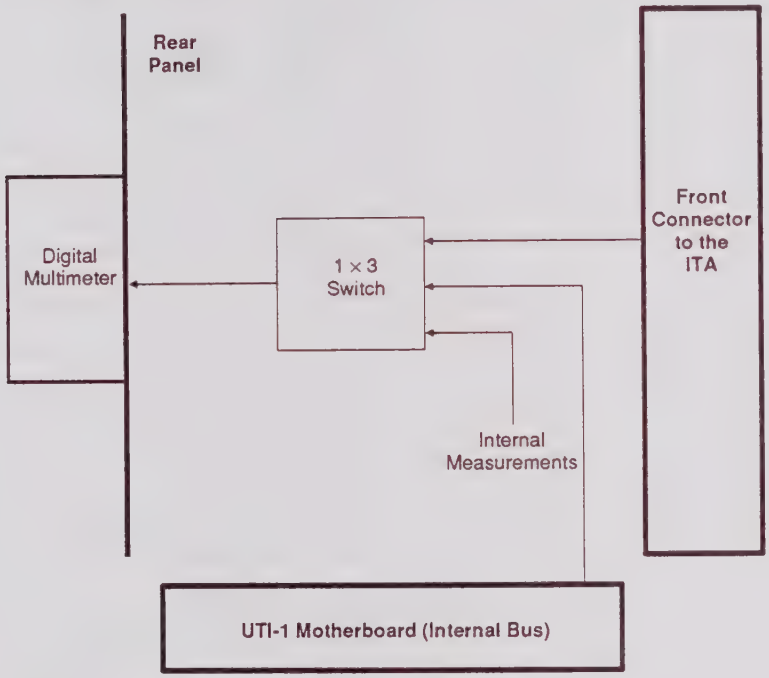


Figure 3.1.5 Digital Multimeter Bus Connections

3.1.6 Coaxial Connections

Rear panel BNC coaxial connectors, Bu11 and Bu12, may only be connected to the UTI-1 motherboard. These connections are made through a set of relay contacts; therefore they can only be controlled together.

The coaxial ports in conjunction with special modules can be useful for signal monitoring using an oscilloscope or frequency counter.

3.1.7 Signal Flow Chart and Pin Locations

Signal Name	Rear Panel Connector	Signal Direction	Front Connector (to ITA) BU1	Motherboard Connection	Notes
AB1 (+)	BU5	⟷	8	ST2 pin 17A	DMM
AB1 (–)	BU5	⟷	7	ST2 pin 18A	
AB1 (gnd)	BU5		9	ST2 pin 19A	
AB2 (T)	BU6	→ Note 1	5	ST2 pin 20A	Transmit
AB2 (R)	BU6	→ Note 1	4	ST2 pin 21A	
AB2 (gnd)	BU6		6	ST2 pin 22A	
AB3 (T)	BU7	← Note 1	2	ST2 pin 23A	Receive
AB3 (R)	BU7	← Note 1	1	ST2 pin 24A	
AB3 (gnd)	BU7		3	ST2 pin 25A	
AB4 (T)	BU8	⟷	65	ST2 pin 26A	Connect to BU1 with jumper E1-E2
AB4 (R)	BU8	⟷	64	ST2 pin 27A	Connect to BU1 with jumper E3-E4
AB4 (gnd)	BU8	⟷	66	ST2 pin 28A	
AB5 (T)	BU9	⟷	68	ST2 pin 17B	Connect to BU1 with jumper E9-E10
AB5 (R)	BU9	⟷	67	ST2 pin 18B	Connect to BU1 with jumper E11-E12
AB5 (gnd)	BU9	⟷	69	ST2 pin 19B	
AB6 (T)	BU10	⟷	71	ST2 pin 20B	Connect to BU1 with jumper E5-E6
AB6 (R)	BU10	⟷	70	ST2 pin 21B	Connect to BU1 with jumper E7-E8
AB6 (gnd)	BU10	⟷	72	ST2 pin 22B	
	BU11	⟷	no connection	ST2 pin 15A	Coaxial Monitor1
	BU12	⟷	no connection	ST2 pin 15B	Coaxial Monitor2

Note 1: When used in the balanced mode, AB2 and AB3 are bi-directional. When used in the single-ended mode, AB2 (R) and AB3 (R) are grounded and the direction is as shown.

Signal Name	Rear Panel Connector	Signal Direction	Front Connector (to ITA) BU1	Motherboard Connection	Notes
S1 +	BU3 pin E	⟷	25	no connection	
S1 –	BU3 pin F	⟷	88	no connection	
V1 +	BU3 pin A	⟷	26	ST1 pin 6A	Connect to ST 1 with jumper E49-E50
V1 –	BU3 pin B	⟷	89	ST1 pin 6B	Connect to ST 1 with jumper E51-E52
S2 +	BU3 pin J	⟷	23	no connection	
S2 –	BU3 pin H	⟷	86	no connection	
V2 +	BU3 pin D	⟷	24	ST1 pin 7A	Connect to ST 1 with jumper E55-E56
V2 –	BU3 pin C	⟷	87	ST1 pin 7B	Connect to ST 1 with jumper E53-E54
S3 +	BU3 pin M	⟷	20	no connection	
S3 –	BU3 pin R	⟷	83	no connection	
V3 +	BU3 pin K	⟷	21	ST1 pin 8A	Connect to ST 1 with jumper E33-E34
V3 –	BU3 pin L	⟷	84	ST1 pin 8B	Connect to ST 1 with jumper E35-E36
S4 +	BU3 pin W	⟷	18	no connection	
S4 –	BU3 pin T	⟷	81	no connection	
V4 +	BU3 pin S	⟷	19	ST1 pin 9A	Connect to ST 1 with jumper E29-E30
V4 –	BU3 pin N	⟷	82	ST1 pin 9B	Connect to ST 1 with jumper E31-E32
S5 +	BU4 pin E	⟷	15	no connection	
S5 –	BU4 pin F	⟷	78	no connection	
V5 +	BU4 pin A	⟷	16	ST1 pin 10A	Connect to ST 1 with jumper E25-E26
V5 –	BU4 pin B	⟷	79	ST1 pin 10B	Connect to ST 1 with jumper E27-E28
S6 +	BU4 pin J	⟷	13	no connection	
S6 –	BU4 pin H	⟷	76	no connection	
V6 +	BU4 pin D	⟷	14	ST1 pin 11A	Connect to ST 1 with jumper E21-E22
V6 –	BU4 pin C	⟷	77	ST1 pin 11B	Connect to ST 1 with jumper E23-E24

Signal Name	Rear Panel Connector	Signal Direction	Front Connector (to ITA) Bu1	Motherboard Connection	Notes
S7+	BU 4 pin M	⟷	no connection	no connection	
S7–	BU 4 pin R	⟷	no connection	no connection	
V7+	BU 4 pin K	⟷	22	ST1 pin 12A	Connect to ST 1 with jumper E17-E18
V7–	BU 4 pin L	⟷	85	ST1 pin 12B	Connect to ST 1 with jumper E19-E20
S8+	BU 4 pin W	⟷	no connection	no connection	
S8–	BU 4 pin T	⟷	no connection	no connection	
V8+	BU 4 pin S	⟷	17	ST1 pin 13A	Connect to ST 1 with jumper E13-E14
V8–	BU 3 pin N	⟷	80	ST1 pin 13B	Connect to ST 1 with jumper E15-E16
A/V–1	BU 3 pin M	⟷	30	ST1 pin 3A	Connect jumper 10-11 on J1 for Bu 1 or J2 for ST 1
A/V–1R	BU 3 pin R	⟷	93	ST1 pin 3B	Connect jumper 9-12 on J1 for Bu 1 or J2 for ST 1
A/V–2	BU 3 pin K	⟷	32	ST1 pin 1A	Connect jumper 8-13 on J1 for Bu 1 or J2 for ST 1
A/V–2R	BU 3 pin L	⟷	31	ST1 pin 2A	Connect jumper 7-14 on J1 for Bu 1 or J2 for ST 1
A/V-3	BU 3 pin W	⟷	95	ST1 pin 1B	Connect jumper 6-15 on J1 for Bu 1 or J2 for ST 1
A/V–3R	BU 3 pin T	⟷	31	ST1 pin 2A	Connect jumper 5-16 on J1 for Bu 1 or J2 for ST 1
A/V–41	BU 3 pin A	⟷	29	ST 1 pin 4A	Connect jumper 4-17 on J1 for Bu 1 or J2 for ST 1
A/V–42	BU 3 pin E	⟷	92	ST 1 pin 4B	Connect jumper 3-18 on J1 for Bu 1 or J2 for ST 1
A/V–51	BU 4 pin B	⟷	28	ST 1 pin 5A	Connect jumper 2-19 on J1 for Bu 1 or J2 for ST 1
A/V–52	BU 4 pin F	⟷	91	ST 1 pin 5B	Connect jumper 1-20 on J1 for Bu 1 or J2 for ST 1
A/C–1	BU 4 pin J	⟷	10	ST 1 pin 18B	Connect to ST 1 with jumper E39-E40
A/C–2	BU 2 pin K	⟷	12	ST 1 pin 17B	Connect to ST 1 with jumper E45-E46
A/C–3	BU 2 pin M	⟷	75	ST 1 pin 17A	Connect to ST 1 with jumper E47-E48
A/C–4	BU 2 pin W	⟷	11	ST 1 pin 16B	Connect to ST 1 with jumper E43-E44
A/C–5	BU 2 pin N	⟷	74	ST 1 pin 16A	Connect to ST 1 with jumper E41-E42
A/C–6	BU 2 pin S	⟷	73	ST 1 pin 18A	Connect to ST 1 with jumper E37-E38

3.2 Programming

3.2.1 Programming Sheets

Function	A	B	C	D	E	F	G	H
Card Select	X							
DMM not connected		0						
DMM connected to Front Panel [Rel 22]		1						
DMM connected to Motherboard [Rel 23]		2						
DMM connected to Transmit Bus (AB 2) [Rel 1, 24]		3	1					
DMM connected to Receive Bus (AB 3) [Rel 2, 24]		3	2					
DMM connected to Analog Bus (AB 4) [Rel 3, 24]		3	3					
DMM connected to Analog Bus (AB 5) [Rel 4, 24]		3	4					
DMM connected to Analog Bus (AB 6) [Rel 5, 24]		3	5					
DMM connected to progr. Voltage V1 [Rel 6, 24]		3	6					
DMM connected to progr. Voltage V2 [Rel 7, 24]		3	7					
DMM connected to progr. Voltage V3 [Rel 8, 24]		3	8					
DMM connected to progr. Voltage V4 [Rel 9, 24]		3	9					
DMM connected to progr. Voltage V5 [Rel 10, 24]		3	10					
DMM connected to progr. Voltage V6 [Rel 11, 24]		3	11					
DMM connected to progr. Voltage V7 [Rel 12, 24]		3	12					
DMM connected to progr. Voltage V8 [Rel 13, 24]		3	13					
DMM connected to Aux Voltage 1 [Rel 14, 24]		3	14					
DMM connected to Aux Voltage 2 [Rel 15, 24]		3	15					
DMM connected to Aux Voltage 3 [Rel 16, 24]		7	1					
DMM connected to Aux Voltage 4 (AC) [Rel 17, 24]		7	2					
DMM connected to Aux Voltage 5 (DC) [Rel 18, 24]		7	3					

Function	A	B	C	D	E	F	G	H
Card Select	X							
DMM connected to Interval +15 Volt [Rel 19, 24]		7	4					
DMM connected to Interval –15 Volt [Rel 20, 24]		7	5					
DMM connected to Interval +5 Volt [Rel 21, 24]		7	6					
BU11 & BU12 connected to ST1, 15A & 15B [Rel 49]		8						
Xmit and Receive balanced Loop Back [Rel 25, 26]				1				
Xmit unbalanced, Receive balanced Loop Back [Rel 27,28]				6				
Xmit balanced				0				
Receive balanced				0				
Xmit and Receive balanced				0				
Xmit unbalanced [Rel 27, 29, 31]				10	2			
Receive unbalanced [Rel 28, 30, 31]				4	3			
Xmit and Receive unbalanced [Rel 27, 28, 29, 30, 31]				14	4			
Connect V1 to Motherboard and Front Panel [Rel 32]						1		
Connect V2 to Motherboard and Front Panel [Rel 33]						2		
Connect V3 to Motherboard and Front Panel [Rel 34]						4		
Connect V4 to Motherboard and Front Panel [Rel 35]						8		
Connect V5 & V6 to Motherboard and Front Panel [Rel 36, 37]							1	
Connect V7 & V8 to Motherboard and Front Panel [Rel 38, 39]							2	
Connect AC & DC Aux Supply to Motherboard and Front Panel [Rel 40, 41]							4	
Connect +Aux Voltage 1, 2 and 3 to Motherboard and Front Panel [Rel 42, 43, 44]							8	

Function	A	B C D E F	G	H
Card Select	X			
Aux Voltage 4 and 5 combined Output disabled				0
Aux Voltage 4 (AC) & 5 (-DC), separate [Rel 40, 41, 45]			4	1
Aux Voltage 4 (AC) superimposed on 5 (-DC) [Rel 40, 41, 45, 46]			4	3
Aux Voltage 4 (AC) & 5 (+DC), separate [Rel 40, 41, 45, 47]			4	5
Aux Voltage 4 (AC) superimposed on Aux Vol. 5 (+DC) [Rel 40, 41, 45, 46, 47]			4	7
Swap H and L Pins of combined Output [Rel 48]				8

3.2.2 Programming Description

The programming word for the Analog Module contains 8 positions (A through H) and each position has sixteen possible values. These values are 0 to 9 and the ASCII equivalents for 10 to 15, which are :, ;, <, =, >, and ? respectively. Position A is reserved for Card Select. Any or all positions may be assigned with a single programming word.

3.2.2.1 Programming Position A

Position A is used to select the proper card in the UTI-1. The value used in this position depends on which slot the Analog Module is in. When looking at the back of the UTI-1, slot 0 is the rightmost slot and slot 15 is the leftmost slot. Position A must be programmed whenever you wish to program anything on this module. If you do not program this position, the information will never reach this module.

3.2.2.2 Programming Position B

Position B controls the access to the digital multimeter bus. The DMM bus may be connected to the Personality Board, the UTI-1 motherboard, or the internal DMM bus on the Analog Interface Module.

Another function of position B is to complete the connection from the BNC connectors Bu 11 and Bu 12 to the motherboard. (B = 8)

3.2.2.3 Programming Position C

Position C selects the signal or voltage on the Analog Module to be connected to the DMM via the internal DMM bus. This allows nearly all the signals and voltages that pass through the module to be measured. (B must be either 3 or 7.)

3.2.2.4 Programming Position D and E

Position D and E route the Analog Transmit and the Analog Receive signals. Selections are made to complete analog loop back and to switch transmit and/or receive between balanced and single ended.

3.2.2.5 Programming Positions F and G

External voltages from the four power supplies can be connected to both the personality board and the motherboard by programming position F. More than one power supply may be enabled by combining the programming values.

Voltages from four other power supplies may be connected by Position G. Position G also connects the auxiliary voltages to the Personality Board and the UTI-1 motherboard.

3.2.2.6 Programming Position H

Position H, with position G selects how the auxiliary voltages are combined. It also allows the output pins of the combined voltages to be reversed.

3.2.2.7 Reading Card ID

The card ID number can be read back from positions B & C. Since binary number 2^0, 2^1, 2^2, and 2^3 are read back in data position C and binary numbers 2^4, 2^5, 2^6, and 2^7 are read back in data position B, the information in M$ must be converted to a decimal ID number. Since the ASCII characters in each position represent 0 through 15, the result can be treated as a HEX number. In the case of this module, the card ID in HEX and decimal is "03".

Note: The actual characters read back in each data position will be the ASCII characters 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, :, ;, <, =, >, and ? which correspond to the HEX characters 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, and F respectively.

The identification number is read back in the following manner:

1. UTI-1 bus address = 709, 4 bit parallel bus address = 1, card slot = 1 (therefore A = 1)
2. Send the card select number and the command to interrogate positions B and C at the same time.
   Output 709;"W1AH1I1BC"
3. Read back the information from the UTI-1 bus and assign it to a string variable.
   Enter 709;Result$

3.2.3 Programming Example

The following example shows how a programming word may be built using the IEEE-488 Bus Interface and HP 200 or 300 series computer. Please refer to the programming sheets.

1. UTI-1 IEEE bus address = 709, 4 bit parallel bus address = 1, card slot = 1 (therefore A = 1.)

   Programming word so far = OUTPUT 709;"W1AH1...."
2. DMM connected to Receive Bus. B = 3, C = 2

   Programming word so far = OUTPUT 709;"W1AH132..."
3. Transmit bus unbalanced Receive bus unbalanced. D = 14 (character equivalent of 14 =), E = 3

   Programming word so far = OUTPUT 709;"W1AH1323..."
4. Connect V1 and V3 power supplies. F = 1 + 4 = 5

   Programming word so far = OUTPUT 709;"W1AH13235..."
5. Connect auxiliary voltage so the AC is superimposed on the -DC and swap polarity. G =4, H = 3 + 8 = 11 or ;

   Final programming word = OUTPUT 709;"W1AH132354;"

3.3. Circuit Description

3.3.1 4 Bit Parallel Bus

The $\overline{CS}$ ($\overline{Card\ Select}$) input line on St2 pin 50B must be in the low state (0 volts) in order for any communication to occur between the system controller and the module. A 0 volt pulse will occur at this point when the proper number, corresponding to the UTI-1 slot number, is sent in the A position. See section 3.2. for further programming information.

In order for the addressable latch IC's (IC1, IC2, IC3, IC 4) to pass any talk information, the card select low pulse must be felt at pin 14 of each of these IC's. The signal path is IC 8 pin 4 to 6 and IC8 pin 10 to 8. This signal will be passed through IC8 pin 10 when the $\overline{T}$/L ($\overline{talk}$ / listen) pin is low, indicating the talk mode. If a high is on the $\overline{T}$/L line, indicating the listen mode, the card select signal will be blocked at IC8 pin 10.

When the $\overline{T}$/L pin is high, the card select will be passed through IC8 pins 13 and 11. The addressable latch IC5 will be activated by the card select, which activates the latch connected to the listen ports.

Each of the talk latches, IC1, IC2, IC3, and IC4, represents a BCD number. IC1 is for 2^0 or 1; IC2 is for 2^1 or 2; IC3 is for 2^2 or 4; IC4 is for 2^3 or 8. The talk data lines from St2 are connected to pin 13 of the appropriate ICs. This data will be latched to the appropiate output pin. The signals labeled POS 2^0, POS 2^1, and POS 2^2 will determine which data is latched to which output. The following chart will show the relationship between the position and the corresponding output pin.

POS 2^0	POS 2^1	POS 2^2	Output pin	Position
L	L	L	4	A
H	L	L	5	B
L	H	L	6	C
H	H	L	7	D
L	L	H	9	E
H	L	H	10	F
L	H	H	11	G
H	H	H	12	H

Each of the latched outputs are used to set the different relays.

The Listen lines are used to read the card ID. This ID code is generated by IC6. When a low pulse is on pin 19, the MSB nibble corresponding to pins 11, 13, 15, and 17 is selected. This code will be read by the computer as a 0 in the B position. When a low pulse is on pin 1, the LSB nibble corresponding to the ground on pins 6 and 8 and the +5V on pins 2 and 4 is selected. This code will be read by the computer as a 3 in the C position.

3.3.2 Digital Multimeter Interface

The digital multimeter is connected to Bu5 of the module's rear panel. On the Analog Module, this line is connected to a 1 x 3 switch consisting of Rel 22, Rel 23, and Rel 24. Relay 22 connects the digital multimeter to Bu1 (Interchangeable Test Adapter connections) pins 7 and 8. Relay 23 connects the digital multimeter to St2 (UTI-1 motherboard internal bus) pins 17A and 18A. Relay 24 connects the digital multimeter to the Analog Module's internal DMM bus for internal measurements. These relays are enabled via multiplexer IC18. This arrangement allows only one relay to be closed at a time.

Relays on each voltage line and each analog bus line connect to the internal DMM bus. These relays are enabled via multiplexer ICs, IC9 and IC10. This arrangement allows only one relay to be closed at a time, preventing shorting voltages together or connecting voltages to analog signal lines.

3.3.3 General Power Supply Interface

Voltages from 8 general power supplies connect at rear panel connectors Bu3 and Bu4. Each voltage line consists of V+, V-, S+, and S-. V+ and V- are the voltage lines, and S+ and S- are the sense lines. All of these lines can be switched to Bu1 (Interchangeable Test Adapter connection) via Relays 32 through 39. By adding jumpers, the voltage lines can be made available at St1 (motherboard internal bus.) The sense lines are not available at the motherboard internal bus.

Note: In Analog Module Series A through E, the sense lines are not switchable, and the voltage lines are connected permanently to St1. The jumpers do not exist on this series.

Each set of voltage lines can be connected to the internal DMM bus by Relays 6 to 13.

3.3.4 Auxiliary Power Supply Interface

Voltages from the Auxiliary power supplies connect at the rear panel connector Bu2. With the J1 jumpers in place, each power supply can be switched to Bu1 (Interchangeable Test Adapter connection) using Relays 40 through 44. With the J2 jumpers in place, each power supply can be switched to St 1 (motherboard internal bus) using the same relays.

Relays 45, 46, and 47 are used to combine auxiliary voltage 4 and auxiliary voltage 5. This is intended for use where auxiliary voltage 4 is an AC voltage and auxiliary voltage 5 is DC. If actuated, Relay 48 reverses the pins of the combined voltage output.

Auxiliary Voltage AC and -DC

When Ringing Voltage AC & -DC is programmed, Relays 40, 41, and 45 are energized. Relays 40 and 41 connect auxiliary voltage 4 and auxiliary voltage 5. Relay 45 connects one side of the AC voltage (auxiliary voltage 42) to ground. The other side of the AC voltage (auxiliary voltage 41) is connected to Bu1 pin 27 via the non energized contacts of Relay 48. The negative DC (auxiliary voltage 52) is connected to Bu1 pin 90 via the non-energized contacts of Relays 47, 46, and 48. The positive DC (auxiliary voltage 51) is connected to ground via the energized contacts of Relay 45 and the non-energized contacts of Relay 47.

Auxiliary Voltage AC Superimposed on -DC

When Auxiliary Voltage AC Superimposed on -DC is programmed, Relays 40, 41, 45, and 46 are energized. Relays 40 and 41 connect auxiliary voltage 4 and auxiliary voltage 5. One side of the AC voltage (auxiliary voltage 41) is connected to Bu1 pin 27 via the non-energized contacts of Relay 48. The other side of the AC voltage (auxiliary voltage 42) is connected to -DC (auxiliary voltage 52 via the energized contacts of Relays 45 and 46 and the non-energized contacts of Relay 47. The positive DC (auxiliary voltage 51) is connected to ground via the energized contacts of Relay 45 and the non-energized contacts of Relay 47. Bu1 pin 90 is connected to ground via the non-energized contacts of Relay 48 and the energized contacts of Relay 46.

Auxiliary Voltage AC and +DC

When Auxiliary Voltage AC & -DC is programmed, Relays 40, 41, 45, and 47 are energized. Relays 40 and 41 connect auxiliary voltage 4 and auxiliary voltage 5. Relay 45 connects one side of the AC voltage (auxiliary voltage 42) to ground. The other side of the AC voltage (auxiliary voltage 41) is connected to Bu1 pin 27 via the non-energized contacts of Relay 48. The positive DC (auxiliary voltage 51) is connected to Bu1 pin 90 via the energized contacts of Relays 47, and the non-energized contacts of Relays 46 and 48. The negative DC (auxiliary voltage 52) is connected to ground via the energized contacts of Relay 47.

Auxiliary Voltage AC Superimposed on +DC

When Auxiliary Voltage AC Superimposed on -DC is programmed, Relays 40, 41, 45, 46, and 47 are energized. Relays 40 and 41 connect auxiliary voltage 4 and auxiliary voltage 5. One side of the AC voltage (auxiliary voltage 41) is connected to Bu 1 pin 27 via the non-energized contacts of Relay 48. The other side of the AC voltage (auxiliary voltage 42) is connected to positive DC (auxiliary voltage 51) via the energized contacts of Relays 45, 46 and 47. The negative DC (auxiliary voltage 52) is connected to ground via the energized contacts of Relay 45 and the non-energized contacts of Relay 47. Bu1 pin 90 is connected to ground via the non-energized contacts of Relay 48 and the energized contacts of Relay 46.

3.3.5 Analog Bus 2 (Transmit)

Analog Bus AB 2 connects via the TF connector Bu6. The default condition of Relays 25, 27, and 29 is to connect this signal, balanced, directly to Bu1 (Interchangeable Test Adapter (ITA) connection) and to St2 (motherboard internal bus.)

Bu6 may be connected to Bu7 by activating Relays 25 and 26. This setup is called the Transmit and Receive Balanced Loop Back.

Relay 27 connects the Balanced signal from Bu6 to the balanced to single-ended amplifier consisting of op amp IC20. The input of IC20 is terminated with R4 600Ω. Diodes D1 through D4 provide overvoltage protection. This amplifier provides a 6 dB overall gain. If activated, Relay 29 connects the single-ended signal to the T (tip) connection of Bu1 (Interchangeable Test Adapter connection) and St2 (motherboard internal bus.) The R (ring) pin at both connectors is connected to ground.

The single-ended amplifier output can be looped back to Bu7 through single-ended to balanced amplifier (IC19) by energizing Relay 28 and not energizing Relay 31. This setup is called the Transmit Unbalanced and Received Balanced Loop Back.

By energizing Relay 1, the AB2 signal at Bu1 and St2 is connected to the internal DMM Bus. If Relay 24 is energized, AB2 can be monitored by a DMM at the rear panel jack Bu5.

3.3.6 Analog Bus 3 (Receive)

Analog Bus AB 3 connects to the test system via connector Bu7. The default connection of Relays 30, 28, and 26 route the signal between Bu1 (Interchangeable Test Adapter connection) and St2 (motherboard internal bus) to the connector Bu7.

For applications where AB3 passes a signal to the test system and comes from a low impedance source, Relays 30 and 31 connect this single-ended signal to the single-ended to balanced amplifier IC19. This converts the signal to 600Ω balanced at the same level as the input signal. R19 and R20 provide the 600Ω impedance from the output of the amplifier. Relay 28 must be activated to pass the output of this circuit to Bu7.

By energizing Relay 2, the AB2 signal at Bu1 and St2 is connected to the internal DMM Bus. If Relay 24 is energized, AB2 can be monitored by a DMM at the rear panel jack Bu5.

3.3.7 Spare Analog Busses 4, 5, and 6

AB 4, 5, and 6 are connected to the test system via rear panel connectors Bu8, Bu9, and Bu10 respectively. These lines are connected directly to St2 (motherboard internal bus) and are not switchable. By adding jumpers to pins E1 to E2, E3 to E4, E9 to E10, E11 to E12, E5 to E6, and E7 to E8, these busses are available at Bu 1 (Interchangeable Test Adapter connections.)

By energizing Relays 3, 4, or 5, the spare analog bus signals can be connected to the internal DMM Bus. If Relay 24 is energized, these signals can be monitored by a DMM at the rear panel jack Bu5.

3.3.8 Coaxial Monitor Busses

Coaxial Monitor Busses Bu11 and Bu12 are connected to St2 (motherboard internal bus) via Relay 49. These lines cannot be connected to the DMM Bus.

GENERAL SUPPLY VOLTAGES

SEE GENERAL SUPPLY VOLTAGES INFORMATION

GENERAL SUPPLY VOLTAGES

INTERNAL DMM BUS

NOTE 1

NOTE 1

DMM

TRANSMIT

RECEIVE

PIN U : BU2

PIN P : BU2

4x1N4448

6dB GAIN

IC20 LF353/2

IC20 LF353/1

IC19

LF353/2

LF353/1

GENERAL SUPPLY VOLTAGES INFORMATION:

A) FOR SERIES A&B: ALL GEN SUPPLY VOLTAGE INPUTS.

B) FOR SERIES C&D: SAME AS SHOWN, EXCEPT PINS 4&5 ; 10&11 ARE SHORTED TOGETHER.

C) FOR SERIES D: SAME AS SERIES C&D, EXCEPT RELAYS 32 THRU 39 ARE NOT INSTALLED.

D) FOR SERIES F: SAME AS SHOWN.

NOTE:

1) FOR FUTURE USE, PINS 33 THROUGH 63, BU1 ARE NOT AVAILABLE IN THIS SERIES.

TO REL 3, PIN4 (PAGE 3)

TO REL 3, PIN13 (PAGE 3)

THIS DRAWING IS OUR PROPERTY.
IT IS NOT TO BE COPIED OR USED
WITHOUT THE WRITTEN CONSENT OF:
WANDEL & GOLTERMANN, INC.

	DATE	NAME
DRAWN	29-7-87	GARRETT
CHKD		
APPRVD		
REPLACES		
REPLCD BY		

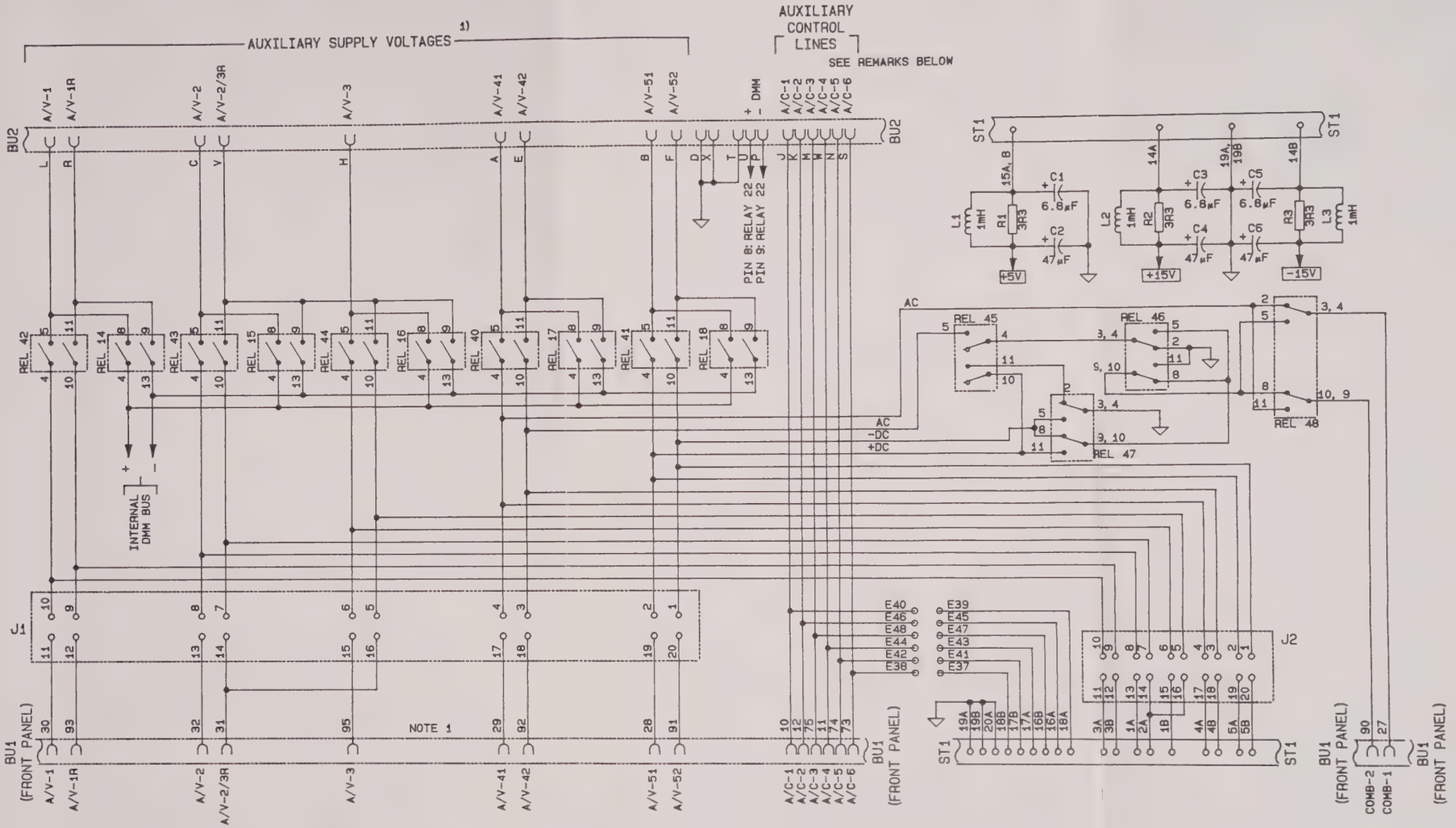
REV	ECN-NO	DATE	NAME
1	NEW	29-7-87	L M G
2	87-157	10NOV87	L M G
3	87-183	2DEC87	M T S
4	88-010	03FEB88	L M G
5	88-056	08APR88	L M G

ANALOG MODULE

SERIES A...

9537-7503.01 /B

PG 1 OF 3



NOTE:
1) FOR FUTURE USE PINS 33 THROUGH 63 BU1 ARE NOT AVAILABLE IN THIS SERIES.

REMARKS:

1) FOR AMS-964 APPLICATIONS:

A/V-1 = +75 VOLTS
A/V-1R = +75 VOLTS RETURN
A/V-2 = +150 VOLTS
A/V-3 = -150 VOLTS
A/V-2/3R = +/-150 VOLT RETURN

A/V-41 = RINGING AC-H
A/V-42 = RINGING AC-L
A/V-51 = RINGING DC+
A/V-52 = RINGING DC-
COMB-1 = RINGING AC/DC COMBINED - H
COMB-2 = RINGING AC/DC COMBINED - L

A/C-1 = INTERLOCK
A/C-2 = ZERO CROSSING (+) POS. IN
A/C-3 = ZERO CROSSING (-) NEG. IN
A/C-4 = ZERO CROSSING LOW LEVEL IN
A/C-5 = ZERO CROSSING OUT
A/C-6 = SUMMING AMP. OUT

GROUND INFO:

FOR SERIES D...

ST1 GND PINS: 19A, 19B, 24A, 26A, 27B, 32A, 37B, 41B, 42A, 43B, 44A, 45B, 46A, 47B, 48A, 49B

ST2 GND PINS: 8A, 9B, 14A, 16A, 16B

FOR SERIES A THRU D; EXCEPT WITH MODIFICATION 253B: ADDITIONAL GROUNDS ARE:

ST1 GND PINS: 20A, 21B, 22A, 23B, 25B, 28A, 29B, 30A, 31B, 34A, 33B, 35A, 26A, 50A

ST2 GND PINS: 1B, 2A, 3B, 4A, 5B, 6A, 7B, 10A, 11B, 12A, 13B

REV	ECN-NO	DATE	NAME
1	NEW	27-7-87	L M G
2	87-157	10NOV87	L M G
3	87-183	2DEC87	M T S
4	88-010	03FEB88	L M G
5	88-056	08APR88	L M G

	DATE	NAME
DRAWN	2 DEC 87	GARRETT
CHKD	26 Apr 88	E Magga
APPRVD		
REPLACES		
REPLCD BY		

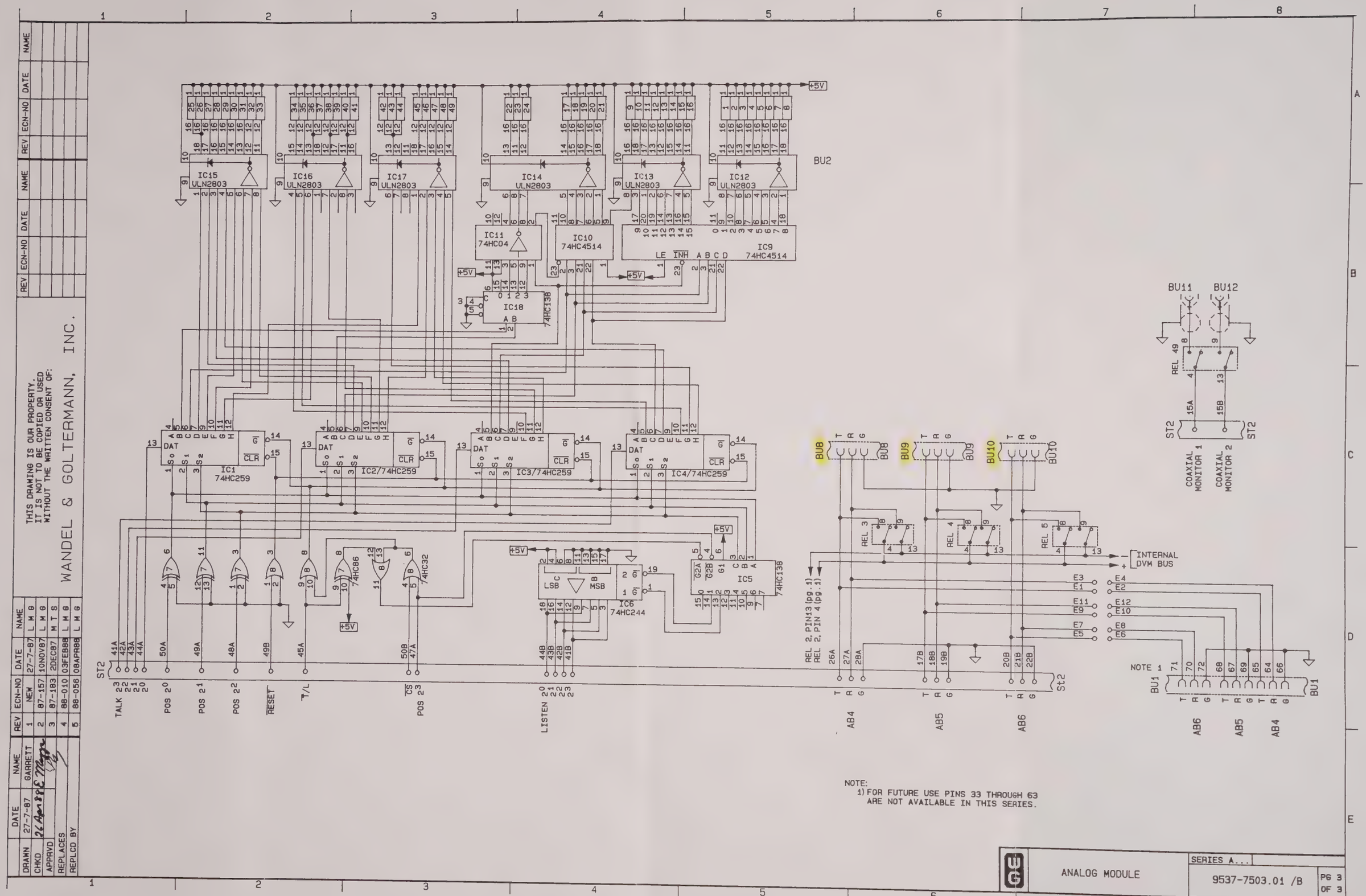
THIS DRAWING IS OUR PROPERTY. IT IS NOT TO BE COPIED OR USED WITHOUT THE WRITTEN CONSENT OF:
WANDEL & GOLTERMANN, INC.

ANALOG MODULE

SERIES A...

9537-7503.01 /B

PG 2 OF 3



NOTE:
1) FOR FUTURE USE PINS 33 THROUGH 63 ARE NOT AVAILABLE IN THIS SERIES.

THIS DRAWING IS OUR PROPERTY. IT IS NOT TO BE COPIED OR USED WITHOUT THE WRITTEN CONSENT OF:

WANDEL & GOLTERMANN, INC.

REV	ECN-NO	DATE	NAME
1	NEW	27-7-87	L M G
2	87-157	10NOV87	L M G
3	87-183	2DEC87	M T S
4	88-010	03FEB88	L M G
5	88-056	08APR88	L M G

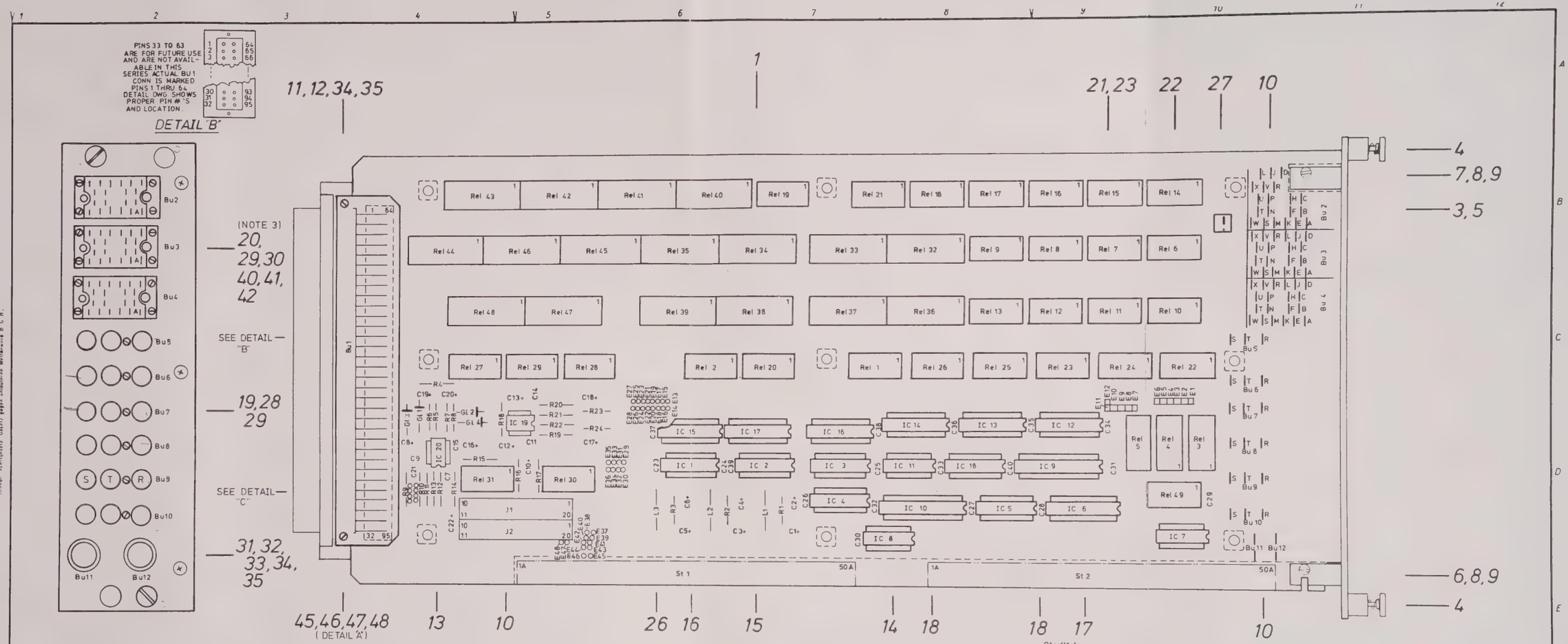
	DATE	NAME
DRAWN	27-7-87	GARRETT
CHKD	26 Apr 88	E Mayer
APPRVD		
REPLACES		
REPLCD BY		

ANALOG MODULE

SERIES A...

9537-7503.01 /B

PG 3 OF 3



NOTES:

1. AREAS WITHIN DOTTED LINES MUST BE SOLDERMASKED USING ITEM 24 OR ITEM 25.
2. LETTER DESIGNATIONS BY SOLDER TERMS FOR Bu2,3 & 4 REFER TO PINS ON CONNECTOR.
3. KEY POSITIONS FOR SMALL AND LARGE PINS ARE: Bu2; Sm. 3 / Lrg. 2
   Bu3; Sm. 2 / Lrg. 2
   Bu4; Sm. 4 / Lrg. 2
4. RELAY 32 THRU 39 NOT USED ON SERIES E.

Oberfläche

Ausgabe	Änderung	Tag	Name
7	ECN# 88-056	8 Apr 88	Les G.
6	ECN# 87-149	12-10-88	M.E.M.
5	ECN# 87-148	10-14-88	M.E.M.
4	ECN# 87-147	10-16-88	M.E.M.
3	ECN# 87-135	10-5-87	M.E.M.
2	ECN# 87-049	5-10-87	[illegible]
1	New	2-4-87	Les G.

Freimaßtoleranzen. WN 51/3/1

	Tag	Name
Bearb	2-APR 87	Les Garcia
Gepr.	2 APR 87	Sanjay Dj.
Norm.		

Wandel u. Goltermann Reutlingen

Halbzeug und Werkstoffe

Benennung: ANALOG MODULE

Maßstab: 1/1

9537-7003.00 /34

Ersatz für: ~

Erstm. Verwdg: ~

WANDEL & GOLTERMANN TECHNOLOGIES, INC.

ANALOG INTERFACE MODULE

BN 9537 ********** LIST OF REPLACEABLE PARTS ********** SERIES: ALL

DATE: Jan 8, 1990

DIAG	REF	ITEM	QTY	PART NUMBER	DESCRIPTION	STOCK LOCATION	VERS/OPT	SERIES STRT	SERIES END	SUBASSEMBLY 9537-XXXX	SUBASSEMBLY CODE
							00 03			7003	S
		0	0	9537-7003.004	ANALOG MODULE		00 03			7003	A
		1	1	9537-7003.020	PC BOARD MACHINED		00 03			7003	
		3	1	9537-7003.059	PANEL REAR MARKED		00 03			7003	M
		5	2	0000-2911.029	LABEL SERIAL ABC		00 03			7003	
		6	1	9537-7001.064	BLOCK PANEL MTG 1		00 03			7003	
		7	2	9537-7001.080	BLOCK PANEL MTG 2		00 03			7003	
		10	122	0000-2901.026	TERM SOLD WN34/5/8		00 03			7003	
		21	1		HEADR STR AU M1X36P	XX03-0375.00	00 03			7003	
		22	0		HEADR STR AU M1X36P	XX03-0375.00	00 03			7003	
		23	0		HEADR STR AU M1X36P	XX03-0375.00	00 03			7003	
		26	3		TUBNG SHRNK 1/4" BLK	XX31-0005.00	00 03			7003	
		27	1	0001-0072.460	LABEL YEL/BLK C-MOS		00 03			7003	
		30	60		CONTACT W/SOLDER EYE	XX03-0380.00	00 03			7003	
		31	2		LUG SOLDER ID10X22MM	XX27-0035.00	00 03			7003	
		34	32		RECEPT PIN ANG ROW#3	XX03-0518.00	00 03	D		7003	
		35	32		RECEPT PIN ANG ROW#1	XX03-0517.00	00 03	D		7003	
		45	1	9537-7003.062	PLATE HIGH VOLTAGE		00 03	C		7003	
		46	1		LABEL DANGER HI VO S	XX21-0044.00	00 03	C		7003	
03	BU	1	1		CONN ANG PC MT F64P	XX03-0521.00	00 03		C	7003	
03	BU	1	1	9537-0000.101	CONN MODIFIED 64P		00 03	D		7003	M
03	BU	2	1		CONN PNL LK NUT M20P	XX03-0376.00	00 03			7003	
03	BU	3	1		CONN PNL LK NUT M20P	XX03-0376.00	00 03			7003	
03	BU	4	1		CONN PNL LK NUT M20P	XX03-0376.00	00 03			7003	
03	BU	5	1	0000-3713.006	JACK S280 TF F39 PNL		00 03			7003	
03	BU	6	1	0000-3713.006	JACK S280 TF F39 PNL		00 03			7003	
03	BU	7	1	0000-3713.006	JACK S280 TF F39 PNL		00 03			7003	
03	BU	8	1	0000-3713.006	JACK S280 TF F39 PNL		00 03			7003	
03	BU	9	1	0000-3713.006	JACK S280 TF F39 PNL		00 03			7003	
03	BU	10	1	0000-3713.006	JACK S280 TF F39 PNL		00 03			7003	
03	BU	11	1	0001-0032.628	CONN BNC PANEL FEM		00 03			7003	
03	BU	12	1	0001-0032.628	CONN BNC PANEL FEM		00 03			7003	
03	C	1	1		C-ELYT TA 6.8U10%35V	XX32-0086.00	00 03			7003	
03	C	2	1		C-ELYT TA 47u 10%20V	XX32-0096.00	00 03			7003	
03	C	3	1		C-ELYT TA 6.8U10%35V	XX32-0086.00	00 03			7003	
03	C	4	1		C-ELYT TA 47u 10%20V	XX32-0096.00	00 03			7003	

WANDEL & GOLTERMANN TECHNOLOGIES, INC.

ANALOG INTERFACE MODULE

BN 9537 ********** LIST OF REPLACEABLE PARTS ********** SERIES: ALL DATE: Jan 8, 1990

DIAG	REF	ITEM	QTY	PART NUMBER	DESCRIPTION	STOCK LOCATION	VERS/OPT	SERIES STRT	SERIES END	SUBASSEMBLY 9537-XXXX	SUBASSEMBLY CODE
03	C	5	1		C-ELYT TA 6.8U10%35V	XX32-0006.00	00 03				7003
03	C	6	1		C-ELYT TA 47u 10%20V	XX32-0096.00	00 03				7003
03	C	7	1	0001-0004.119	C-CER 4.7P +-.25P63V		00 03				7003
03	C	8	1		C-ELYT TA 47u 10%20V	XX32-0096.00	00 03				7003
03	C	9	1		C-CER 10 N 10% 50V	XX02-0270.00	00 03				7003
03	C	10	1		CAP TANT 2.2uF 35V	XX32-0084.00	00 03				7003
03	C	11	1		C-CER 10 N 10% 50V	XX02-0270.00	00 03				7003
03	C	12	1		C-ELYT TA 47u 10%20V	XX32-0096.00	00 03				7003
03	C	13	1		C-ELYT TA 47u 10%20V	XX32-0096.00	00 03				7003
03	C	14	1		C-CER 10 N 10% 50V	XX02-0270.00	00 03				7003
03	C	15	1		C-CER 10 N 10% 50V	XX02-0270.00	00 03				7003
03	C	16	1		C-ELYT TA 47u 10%20V	XX32-0096.00	00 03				7003
03	C	17	1	0001-0041.059	C-ELYT TA 47U 6.3V		00 03				7003
03	C	18	1	0001-0041.059	C-ELYT TA 47U 6.3V		00 03				7003
03	C	19	1		C TANT .68uF 10% 35V	XX32-0107.00	00 03				7003
03	C	20	1		C TANT .68uF 10% 35V	XX32-0107.00	00 03				7003
03	C	21	1	0001-0004.119	C-CER 4.7P +-.25P63V		00 03				7003
03	C	22	1	0001-0041.059	C-ELYT TA 47U 6.3V		00 03				7003
03	C	23	1	0000-7632.659	C-CER 100N 10% 50V		00 03				7003
03	C	24	1	0000-7632.659	C-CER 100N 10% 50V		00 03				7003
03	C	25	1	0000-7632.659	C-CER 100N 10% 50V		00 03				7003
03	C	26	1	0000-7632.659	C-CER 100N 10% 50V		00 03				7003
03	C	27	1	0000-7632.659	C-CER 100N 10% 50V		00 03				7003
03	C	28	1	0000-7632.659	C-CER 100N 10% 50V		00 03				7003
03	C	29	1	0000-7632.659	C-CER 100N 10% 50V		00 03				7003
03	C	30	1	0000-7632.659	C-CER 100N 10% 50V		00 03				7003
03	C	31	1	0000-7632.659	C-CER 100N 10% 50V		00 03				7003
03	C	32	1	0000-7632.659	C-CER 100N 10% 50V		00 03				7003
03	C	33	1	0000-7632.659	C-CER 100N 10% 50V		00 03				7003
03	C	34	1	0000-7632.659	C-CER 100N 10% 50V		00 03				7003
03	C	35	1	0000-7632.659	C-CER 100N 10% 50V		00 03				7003
03	C	36	1	0000-7632.659	C-CER 100N 10% 50V		00 03				7003
03	C	37	1	0000-7632.659	C-CER 100N 10% 50V		00 03				7003
03	C	38	1	0000-7632.659	C-CER 100N 10% 50V		00 03				7003
03	C	39	1	0000-7632.659	C-CER 100N 10% 50V		00 03				7003
03	C	40	1	0000-7632.659	C-CER 100N 10% 50V		00 03				7003

WANDEL & GOLTERMANN TECHNOLOGIES, INC.

ANALOG INTERFACE MODULE

BN 9537 ********** LIST OF REPLACEABLE PARTS ********** SERIES: ALL DATE: Jan 8, 1990

DIAG	REF	ITEM	QTY	PART NUMBER	DESCRIPTION	STOCK LOCATION	VERS/OPT	SERIES STRT	SERIES END	SUBASSEMBLY 9537-XXXX CODE
03	GL	1	1	0001-0018.493	DIODE 1N4448		00 03			7003
03	GL	2	1	0001-0018.493	DIODE 1N4448		00 03			7003
03	GL	3	1	0001-0018.493	DIODE 1N4448		00 03			7003
03	GL	4	1	0001-0018.493	DIODE 1N4448		00 03			7003
03	IC	1	1	0000-7597.590	IC MOS 74HC259 D16		00 03			7003
03	IC	2	1	0000-7597.590	IC MOS 74HC259 D16		00 03			7003
03	IC	3	1	0000-7597.590	IC MOS 74HC259 D16		00 03			7003
03	IC	4	1	0000-7597.590	IC MOS 74HC259 D16		00 03			7003
03	IC	5	1	0000-7597.309	IC MOS 74HC138 D16		00 03			7003
03	IC	6	1	0000-7623.192	IC MOS 74HCT244 D20		00 03			7003
03	IC	7	1	0000-7597.244	IC MOS 74HC86 D14		00 03			7003
03	IC	8	1	0000-7597.176	IC MOS 74HC32 D14		00 03			7003
03	IC	9	1	0000-7597.930	IC MOS 74HC4514 D24		00 03			7003
03	IC	10	1	0000-7597.930	IC MOS 74HC4514 D24		00 03			7003
03	IC	11	1	0000-7597.105	IC MOS 74HC04 D14		00 03			7003
03	IC	12	1	0000-7579.657	IC DRVR ULN2803A D18		00 03			7003
03	IC	13	1	0000-7579.657	IC DRVR ULN2803A D18		00 03			7003
03	IC	14	1	0000-7579.657	IC DRVR ULN2803A D18		00 03			7003
03	IC	15	1	0000-7579.657	IC DRVR ULN2803A D18		00 03			7003
03	IC	16	1	0000-7579.657	IC DRVR ULN2803A D18		00 03			7003
03	IC	17	1	0000-7579.657	IC DRVR ULN2803A D18		00 03			7003
03	IC	18	1	0000-7597.309	IC MOS 74HC138 D16		00 03			7003
03	IC	19	1	0000-7676.055	IC OP-AMP/2 LF353 D8		00 03			7003
03	IC	20	1	0000-7676.055	IC OP-AMP/2 LF353 D8		00 03			7003
03	L	1	1	0001-0042.757	L-FERRITE 27U HORIZ		00 03			7003
03	L	2	1	0001-0042.757	L-FERRITE 27U HORIZ		00 03			7003
03	L	3	1	0001-0042.757	L-FERRITE 27U HORIZ		00 03			7003
03	R	1	1	0000-7629.743	R-MF 3.32R 2% 2W4		00 03			7003
03	R	2	1	0000-7629.743	R-MF 3.32R 2% 2W4		00 03			7003
03	R	3	1	0000-7629.743	R-MF 3.32R 2% 2W4		00 03			7003
03	R	4	1		MF 602 .1% 1/4W	XX00-0601.00	00 03			7003
03	R	5	1	0000-7633.991	R-MF 200K 1% 2W4		00 03			7003
03	R	6	1	0000-7633.991	R-MF 200K 1% 2W4		00 03			7003
03	R	7	1	0000-7633.991	R-MF 200K 1% 2W4		00 03			7003
03	R	8	1	0000-7633.991	R-MF 200K 1% 2W4		00 03			7003
03	R	9	1	0000-7629.743	R-MF 3.32R 2% 2W4		00 03			7003

WANDEL & GOLTERMANN TECHNOLOGIES, INC.

ANALOG INTERFACE MODULE

SERIES: ALL

BN 9537 ********** LIST OF REPLACEABLE PARTS ********** DATE: Jan 8, 1990

DIAG	REF	ITEM	QTY	PART NUMBER	DESCRIPTION	STOCK LOCATION	VERS/OPT	SERIES STRT	SERIES END	SUBASSEMBLY 9537-XXXX	CODE
03	R	10	1	0000-7559.091	R-MF 5.23K 0.1% 207		00 03				7003
03	R	11	1	0000-7559.091	R-MF 5.23K 0.1% 207		00 03				7003
03	R	12	1	0000-7559.091	R-MF 5.23K 0.1% 207		00 03				7003
03	R	13	1	0000-7559.091	R-MF 5.23K 0.1% 207		00 03				7003
03	R	14	1	0000-7629.743	R-MF 3.32R 2% 204		00 03				7003
03	R	15	1	0000-7607.244	R-MF 56.2K 1% 204		00 03				7003
03	R	16	1	0000-7633.991	R-MF 200K 1% 204		00 03				7003
03	R	17	1	0000-7633.991	R-MF 200K 1% 204		00 03				7003
03	R	18	1	0000-7633.991	R-MF 200K 1% 204		00 03				7003
03	R	19	1		MF 300 .1% 1/4W	XX00 0599.00	00 03				7003
03	R	20	1		MF 300 .1% 1/4W	XX00 0599.00	00 03				7003
03	R	21	1	0000-7543.492	R-MF 9.09K 0.1% 207		00 03				7003
03	R	22	1	0000-7543.492	R-MF 9.09K 0.1% 207		00 03				7003
03	R	23	1	0000-7633.991	R-MF 200K 1% 204		00 03				7003
03	R	24	1	0000-7633.991	R-MF 200K 1% 204		00 03				7003
03	REL	1	1		RELAY DS-2ES-DC5V	XX07 0042.00	00 03				7003
03	REL	2	1		RELAY DS-2ES-DC5V	XX07 0042.00	00 03				7003
03	REL	3	1		RELAY DS-2ES-DC5V	XX07 0042.00	00 03				7003
03	REL	4	1		RELAY DS-2ES-DC5V	XX07 0042.00	00 03				7003
03	REL	5	1		RELAY DS-2ES-DC5V	XX07 0042.00	00 03				7003
03	REL	6	1		RELAY DS-2ES-DC5V	XX07 0042.00	00 03				7003
03	REL	7	1		RELAY DS-2ES-DC5V	XX07 0042.00	00 03				7003
03	REL	8	1		RELAY DS-2ES-DC5V	XX07 0042.00	00 03				7003
03	REL	9	1		RELAY DS-2ES-DC5V	XX07 0042.00	00 03				7003
03	REL	10	1		RELAY DS-2ES-DC5V	XX07 0042.00	00 03				7003
03	REL	11	1		RELAY DS-2ES-DC5V	XX07 0042.00	00 03				7003
03	REL	12	1		RELAY DS-2ES-DC5V	XX07 0042.00	00 03				7003
03	REL	13	1		RELAY DS-2ES-DC5V	XX07 0042.00	00 03				7003
03	REL	14	1		RELAY DS-2ES-DC5V	XX07 0042.00	00 03				7003
03	REL	15	1		RELAY DS-2ES-DC5V	XX07 0042.00	00 03				7003
03	REL	16	1		RELAY DS-2ES-DC5V	XX07 0042.00	00 03				7003
03	REL	17	1		RELAY DS-2ES-DC5V	XX07 0042.00	00 03				7003
03	REL	18	1		RELAY DS-2ES-DC5V	XX07 0042.00	00 03				7003
03	REL	19	1		RELAY DS-2ES-DC5V	XX07 0042.00	00 03				7003
03	REL	20	1		RELAY DS-2ES-DC5V	XX07 0042.00	00 03				7003
03	REL	21	1		RELAY DS-2ES-DC5V	XX07 0042.00	00 03				7003

WANDEL & GOLTERMANN TECHNOLOGIES, INC.

ANALOG INTERFACE MODULE

SERIES: ALL

BN 9537 ********** LIST OF REPLACEABLE PARTS ********** DATE: Jan 8, 1990

DIAG	REF	ITEM	QTY	PART NUMBER	DESCRIPTION	STOCK LOCATION	VERS/OPT	SERIES STRT	SERIES END	SUBASSEMBLY 9537-XXXX	CODE
03	REL	22	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 03				7003
03	REL	23	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 03				7003
03	REL	24	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 03				7003
03	REL	25	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 03				7003
03	REL	26	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 03				7003
03	REL	27	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 03				7003
03	REL	28	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 03				7003
03	REL	29	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 03				7003
03	REL	30	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 03				7003
03	REL	31	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 03				7003
03	REL	32	1	0000-7568.330	RELAY PC MT 5V 2A2B		00 03		D		7003
03	REL	32	1		RELAY PC 5VDC 4A	XX07-0053.00	00 03	F			7003
03	REL	33	1	0000-7568.330	RELAY PC MT 5V 2A2B		00 03		D		7003
03	REL	33	1		RELAY PC 5VDC 4A	XX07-0053.00	00 03	F			7003
03	REL	34	1	0000-7568.330	RELAY PC MT 5V 2A2B		00 03		D		7003
03	REL	34	1		RELAY PC 5VDC 4A	XX07-0053.00	00 03	F			7003
03	REL	35	1	0000-7568.330	RELAY PC MT 5V 2A2B		00 03		D		7003
03	REL	35	1		RELAY PC 5VDC 4A	XX07-0053.00	00 03	F			7003
03	REL	36	1	0000-7568.330	RELAY PC MT 5V 2A2B		00 03		D		7003
03	REL	36	1		RELAY PC 5VDC 4A	XX07-0053.00	00 03	F			7003
03	REL	37	1	0000-7568.330	RELAY PC MT 5V 2A2B		00 03		D		7003
03	REL	37	1		RELAY PC 5VDC 4A	XX07-0053.00	00 03	F			7003
03	REL	38	1	0000-7568.330	RELAY PC MT 5V 2A2B		00 03		D		7003
03	REL	38	1		RELAY PC 5VDC 4A	XX07-0053.00	00 03	F			7003
03	REL	39	1	0000-7568.330	RELAY PC MT 5V 2A2B		00 03		D		7003
03	REL	39	1		RELAY PC 5VDC 4A	XX07-0053.00	00 03	F			7003
03	REL	40	1	0000-7568.330	RELAY PC MT 5V 2A2B		00 03				7003
03	REL	41	1	0000-7568.330	RELAY PC MT 5V 2A2B		00 03				7003
03	REL	42	1	0000-7568.330	RELAY PC MT 5V 2A2B		00 03				7003
03	REL	43	1	0000-7568.330	RELAY PC MT 5V 2A2B		00 03				7003
03	REL	44	1	0000-7568.330	RELAY PC MT 5V 2A2B		00 03				7003
03	REL	45	1	0000-7568.330	RELAY PC MT 5V 2A2B		00 03				7003
03	REL	46	1	0000-7568.330	RELAY PC MT 5V 2A2B		00 03				7003
03	REL	47	1	0000-7568.330	RELAY PC MT 5V 2A2B		00 03				7003
03	REL	48	1	0000-7568.330	RELAY PC MT 5V 2A2B		00 03				7003
03	REL	49	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 03				7003

Contents **Page**

1. Introduction 1-1
2. Specifications 2-1
   - 2.1. DC Characteristics 2-1
   - 2.2. AC Characteristics 2-1
   - 2.3. Relay Characteristics 2-1
3. Operating Description 3-1
   - 3.1. Detailed Description of Features 3-1
     - 3.1.1 Switching Matrix 3-1
     - 3.1.2 High Fidelity Coupling 3-1
     - 3.1.3 Typical Application 3-2
     - 3.1.4 Input Channel Pin Locations 3-3
     - 3.1.5 Output Channel Pin Locations 3-5
   - 3.2. Programming 3-7
     - 3.2.1 Programming Sheets 3-7
     - 3.2.2 Programming Description 3-15
       - 3.2.2.1 Programming Position A 3-15
       - 3.2.2.2 Programming Position B 3-15
       - 3.2.2.3 Programming Position C 3-15
       - 3.2.2.4 Programming Position D 3-15
       - 3.2.2.5 Programming Position E 3-15
       - 3.2.2.6 Programming Position F 3-16
       - 3.2.2.7 Programming Position G 3-16
       - 3.2.2.8 Programming Position H 3-16
       - 3.2.2.9 Programming Position I 3-16
       - 3.2.2.10 Programming Position J 3-16
       - 3.2.2.11 Programming Position K 3-16
       - 3.2.2.12 Programming Position L 3-16
       - 3.2.2.13 Programming Position M 3-16
       - 3.2.2.14 Programming Position N 3-17
       - 3.2.2.15 Programming Position O 3-17
       - 3.2.2.16 Programming Position P 3-17
       - 3.2.2.17 Reading Card ID 3-17
     - 3.2.3 Programming Example 3-18
   - 3.3. Circuit Description 3-19
     - 3.3.1 4 Bit Parallel Bus 3-19
     - 3.3.2 Relay Drivers 3-20
     - 3.3.3 Relay Matrix 3-20
   - 3.4. Schematic Diagram / Parts List 3-21

6 × 8 Balanced Switching Matrix Description and Operation

1. Introduction

The 6 × 8 Balanced Switching Matrix Module is designed to connect any of the six balanced busses from the Motherboard to any of the eight balanced busses on the front connector. More modules can be added to expand the configuration to 6 × 16, 6 × 24,6 × 32, and so on. All the eight balanced busses going to the front connector can be terminated with resistors, capacitors or a combination of both.

2. Specifications

2.1. DC Characteristics

Maximum power consumption per module

1) Power consumption during normal usage. The six motherboard busses (AB1 through AB6) are connected to six of the Interchangeable Test Adapter output channels. The two remaining output channels are terminated.

	+5 V	+15 V	-15 V	Total
Current (Amps)	1.2	-----	-----	-----
Power (Watts)	6	-----	-----	6

2) Power consumption during minimal usage. All eight Interchangeable Test Adapter output channels are terminated.

	+5 V	+15 V	-15 V	Total
Current (Amps)	0.75	-----	-----	-----
Power (Watts)	3.75	-----	-----	3.75

3) Power consumption with all relays energized. This condition is not typical.

	+5 V	+15 V	-15 V	Total
Current (Amps)	5.0	-----	-----	-----
Power (Watts)	25.0	-----	-----	25.0

2.2. AC Characteristics

Capacitance (including motherboard lines)
- Open Channel . . . . . <45 pf
- Channel to Channel . . . . . <150 pf
- Channel to Ground . . . . . <130 pf

Insertion Loss @ 1 kHz . . . . . ≤0.02 dB*

Frequency Response referenced to 1 KHz
- 0.02 to 100 kHz . . . . . ≤0.05 dB*
- 100 to 620 kHz . . . . . ≤0.50 dB*

Crosstalk (0.02 to 10 kHz) . . . . . ≥95 dB*
- (f ≤ 620 kHz) . . . . . ≥60 dB*

* All measurements with 600Ω termination. Measurements include Motherboard influence.

2.3. Relay Characteristics

Relay contact pull-in time . . . . . 3 msec
Relay contact release time . . . . . 2 msec
Relay carrying current . . . . . .3.0 Amps maximum
Relay switching current . . . . . .2.0 Amps maximum
Relay switching voltage . . . . . 250 Volts
Min. expected life under 30 V DC
and 1 Amp load . . . . . 2×10^6 operations

3. Operating Description

3.1. Detailed Description Of Features

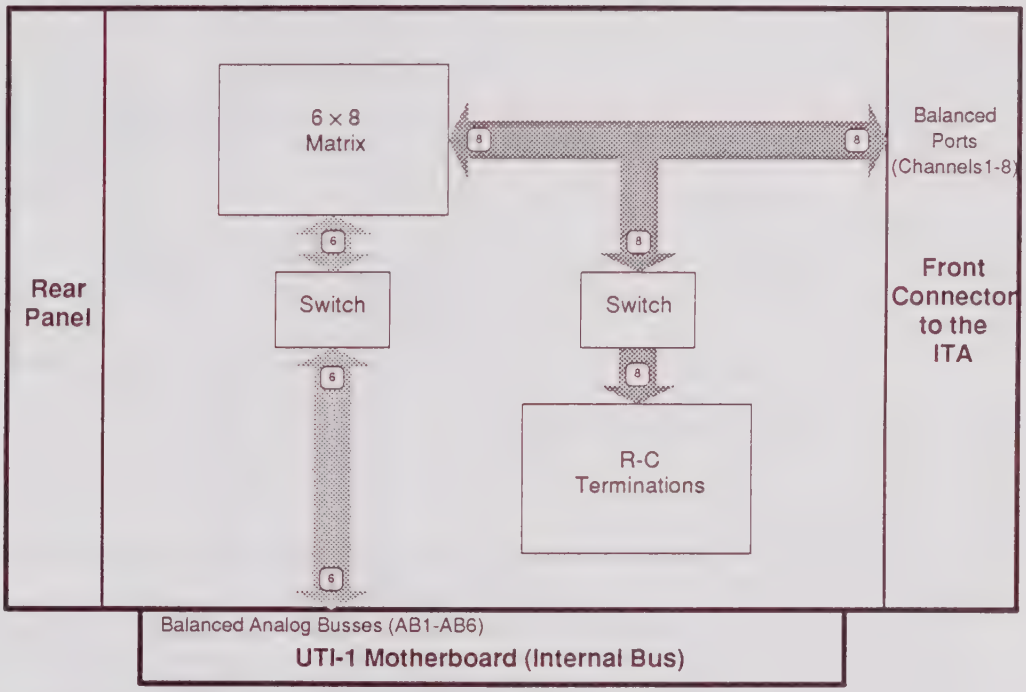


Figure 3.1. Basic Block Diagram

3.1.1 Switching Matrix

The 6 x 8 Balanced Switching Matrix is an extremely reliable and versatile analog switching matrix. A single module allows six balanced busses from the UTI-1 motherboard to establish electrical connection with any of the eight channels connected to the Interchangeable Test Adapter. Figure 3.1. shows a basic block diagram of this module.

3.1.2 High Fidelity Coupling

Each of the eight channels connected to the Interchangeable Test Adapter has access to an RC termination network (see figure 3.1.2). High fidelity coupling of signals in the audio frequency range can be accomplished by terminating those channels which are not selected during the test. The RC terminations are normally 600Ω in series with 2.2μF, but they can be configured to accommodate specific customer requirements.

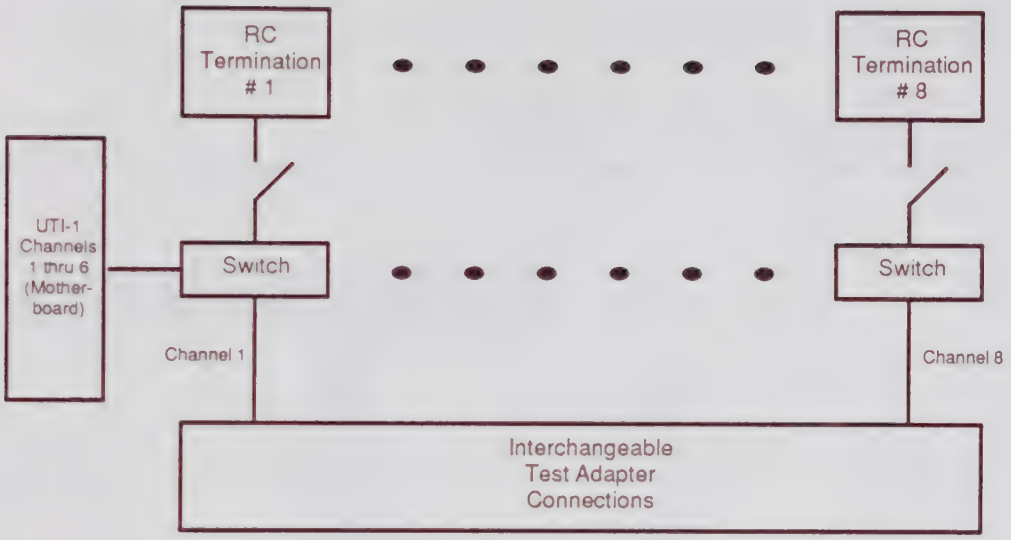


Figure 3.1.2 RC Termination Coupling

3.1.3 Typical Application

Although the 6 × 8 Balanced Switching Matrix has potential for a wide range of applications, a single example will be discussed here for the sake of clarity.

Figure 3.1.2 shows an application in which a signal (stimulus) is fed to the UUT through one of the six channels in the motherboard. A second channel is used for connecting a special bridge, and a third channel is used for connecting a custom termination. The remaining channels are used to monitor and compute the UUT output signal (response).

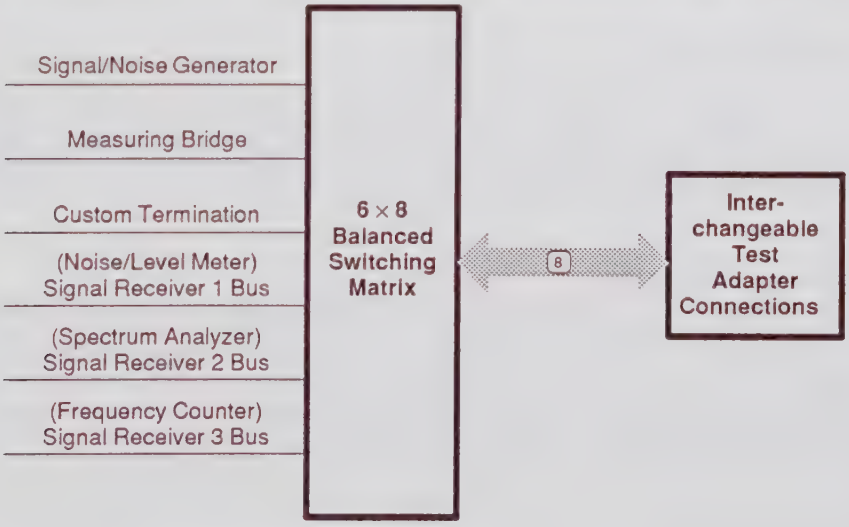


Figure 3.1.3 Analog Signal Monitoring Application

3.1.4 Input Channel Pin Locations

Signal Name		Motherboard Connection St 2	Notes
AB1	(T)	17A	
	(R)	18A	
	(grnd)	19A	
AB2	(T)	20A	
	(R)	21A	
	(grnd)	22A	
AB3	(T)	23A	
	(R)	24A	
	(grnd)	25A	
AB4	(T)	26A	
	(R)	27A	
	(grnd)	28A	
AB5	(T)	17B	
	(R)	18B	
	(grnd)	19B	
AB6	(T)	20B	
	(R)	21B	
	(grnd)	22B	

3.1.5 Output Channel Pin Locations

Signal Name	ITA Connections Bu 1	Notes
CH1 (T)	68	
(R)	67	
(grnd)	69	
CH2 (T)	71	
(R)	70	
(grnd)	72	
CH3 (T)	74	
(R)	73	
(grnd)	75	
CH4 (T)	77	
(R)	76	
(grnd)	78	
CH5 (T)	80	
(R)	79	
(grnd)	81	
CH6 (T)	83	
(R)	82	
(grnd)	84	
CH7 (T)	86	
(R)	85	
(grnd)	87	
CH8 (T)	89	
(R)	88	
(grnd)	90	

3.2. Programming

Before starting any programming for the 6 × 8 Balanced Switching Matrix, the user must first select which input channels connect to which output channels. The input channels are the six analog busses (AB 1 to AB 6) on the UTI-1 motherboard. The output channels are the eight channels connected to the Interchangeable Test Adapter.

After the input to output interconnections are established, the 4 Bit Parallel Bus control word can be assembled using the following programming sheets.

3.2.1 Programming Sheets

Bank "0":

Position	Function	Data	Notes
A	Card Select		
B	Bank Select	0	
C	Input Ch1 not connected to Output Ch1 ... 4	0	1
	Input Ch1 connected to Output Ch1	1	
	Input Ch1 connected to Output Ch2	2	
	Input Ch1 connected to Output Ch3	4	
	Input Ch1 connected to Output Ch4	8	
D	Input Ch1 not connected to Output Ch5 ... 8	0	1
	Input Ch1 connected to Output Ch5	1	
	Input Ch1 connected to Output Ch6	2	
	Input Ch1 connected to Output Ch7	4	
	Input Ch1 connected to Output Ch8	8	
E	Input Ch2 not connected to Output Ch1 ... 4	0	1
	Input Ch2 connected to Output Ch1	1	
	Input Ch2 connected to Output Ch2	2	
	Input Ch2 connected to Output Ch3	4	
	Input Ch2 connected to Output Ch4	8	

Position	Function	Data	Notes
F	Input Ch2 not connected to Output Ch5 ... 8	0	1
	Input Ch2 connected to Output Ch5	1	
	Input Ch2 connected to Output Ch6	2	
	Input Ch2 connected to Output Ch7	4	
	Input Ch2 connected to Output Ch8	8	
G	Input Ch3 not connected to Output Ch1 ... 4	0	1
	Input Ch3 connected to Output Ch1	1	
	Input Ch3 connected to Output Ch2	2	
	Input Ch3 connected to Output Ch3	4	
	Input Ch3 connected to Output Ch4	8	
H	Input Ch3 not connected to Output Ch5 ... 8	0	1
	Input Ch3 connected to Output Ch5	1	
	Input Ch3 connected to Output Ch6	2	
	Input Ch3 connected to Output Ch7	4	
	Input Ch3 connected to Output Ch8	8	
I	Input Ch4 not connected to Output Ch1 ... 4	0	1
	Input Ch4 connected to Output Ch1	1	
	Input Ch4 connected to Output Ch2	2	
	Input Ch4 connected to Output Ch3	4	
	Input Ch4 connected to Output Ch4	8	
J	Input Ch4 not connected to Output Ch5 ... 8	0	1
	Input Ch4 connected to Output Ch5	1	
	Input Ch4 connected to Output Ch6	2	
	Input Ch4 connected to Output Ch7	4	
	Input Ch4 connected to Output Ch8	8	

Position	Function	Data	Notes
K	Input Ch5 not connected to Output Ch1 ... 4	0	1
	Input Ch5 connected to Output Ch1	1	
	Input Ch5 connected to Output Ch2	2	
	Input Ch5 connected to Output Ch3	4	
	Input Ch5 connected to Output Ch4	8	
L	Input Ch5 not connected to Output Ch5 ... 8	0	1
	Input Ch5 connected to Output Ch5	1	
	Input Ch5 connected to Output Ch6	2	
	Input Ch5 connected to Output Ch7	4	
	Input Ch5 connected to Output Ch8	8	
M	Input Ch6 not connected to Output Ch1 ... 4	0	1
	Input Ch6 connected to Output Ch1	1	
	Input Ch6 connected to Output Ch2	2	
	Input Ch6 connected to Output Ch3	4	
	Input Ch6 connected to Output Ch4	8	
N	Input Ch6 not connected to Output Ch5 ... 8	0	1
	Input Ch6 connected to Output Ch5	1	
	Input Ch6 connected to Output Ch6	2	
	Input Ch6 connected to Output Ch7	4	
	Input Ch6 connected to Output Ch8	8	
O	Outputs Ch1 ... 4 not terminated	0	2
	Output Ch1 terminated	1	
	Output Ch2 terminated	2	
	Output Ch3 terminated	4	
	Output Ch4 terminated	8	
P	Outputs Ch5 ... 8 not terminated	0	2
	Output Ch5 terminated	1	
	Output Ch6 terminated	2	
	Output Ch7 terminated	4	
	Output Ch8 terminated	8	

Bank "1":

Position	Function	Data	Notes
A	Card Select		
B	Bank Select	1	
C	Input Ch1-Ch4 not connected to Matrix	0	2
	Input Ch1 connected Matrix	1	
	Input Ch2 connected to Matrix	2	
	Input Ch3 connected to Matrix	4	
	Input Ch4 connected to Matrix	8	
D	Inputs Ch5 and Ch6 not connected to Matrix	0	2
	Input Ch5 connected to Matrix	1	
	Input Ch6 connected to Matrix	2	

Note 1: Other than the specified data is not allowed.

Note 2: If more than one function is desired, add the corresponding rows.

3.2.2 Programming Description

Programming the 6x8 Balanced Switching Matrix is accomplished through a 4 Bit Parallel Bus. This bus uses "W" control blocks for talk operations and "I" control blocks for listen operations (see 4 Bit Parallel Bus section of this manual).

A complete control block for this module contains sixteen positions (A through P) and each position has sixteen possible values. These values are numbers 0 through 9 and the ASCII character equivalents of 10 through 15. The ASCII characters equivalent to 10, 11, 12, 13, 14, and 15 are :, ;, <, =, >, and ? respectively.

3.2.2.1 Programming Position A

Position A is used to select the proper card in the UTI-1. The value used in this position corresponds to the slot number in which the 6x8 Balanced Switching Matrix is located. When looking at the back of the UTI-1, the rightmost location corresponds to slot number 0 and the leftmost location corresponds to slot number 15. If you do not program this position, the information will never reach this module.

3.2.2.2 Programming Position B

Position B is the data Bank Select position. The 6×8 Balanced Switching Matrix has two data banks; these are Bank 0 and Bank 1. Bank 0 is used to control all of the connections within the matrix. Bank 1 is used to connect or disconnect the matrix to the six input channels from the UTI-1 motherboard.

3.2.2.3 Programming Position C

If Bank Select is 0, position C programs the connection between Input Channel 1 and Output Channels 1 through 4.

If Bank Select is 1, the value in position C determines whether Input Channels 1 through 4 are connected to the matrix or not.

3.2.2.4 Programming Position D

If Bank Select is 0, position D programs the connection between Input Channel 1 and Output Channels 5 through 8.

If Bank Select is 1, the value of position C determines whether Input Channels 5 and 6 are connected to the matrix or not.

3.2.2.5 Programming Position E

If Bank Select is 0, the value of position E programs the connection between Input Channel 2 and Output Channels 1 through 4.

Position E can only be programmed when Bank Select = 0.

3.2.2.6 Programming Position F

If Bank Select is 0, position F programs the connection between Input Channel 2 and Output Channels 5 through 8.

Position F can only be programmed when Bank Select = 0.

3.2.2.7 Programming Position G

If Bank Select is 0, position G programs the connection between Input Channel 3 and Output Channels 1 through 4.

Position G can only be programmed when Bank Select = 0.

3.2.2.8 Programming Position H

If Bank Select is 0, position H programs the connection between Input Channel 3 and Output Channels 5 through 8.

Position H can only be programmed when Bank Select = 0.

3.2.2.9 Programming Position I

If Bank Select is 0, position I programs the connection between Input Channel 4 and Output Channels 1 through 4.

Position I can only be programmed when Bank Select = 0.

3.2.2.10 Programming Position J

If Bank Select is 0, position J programs the connection between Input Channel 4 and Output Channels 5 through 8.

Position J can only be programmed when Bank Select = 0.

3.2.2.11 Programming Position K

If Bank Select is 0, position K programs the connection between Input Channel 5 and Output Channels 1 through 4.

Position K can only be programmed when Bank Select = 0.

3.2.2.12 Programming Position L

If Bank Select is 0, position L programs the connection between Input Channel 5 and Output Channels 5 through 8.

Position L can only be programmed when Bank Select = 0.

3.2.2.13 Programming Position M

If Bank Select is 0, position M programs the connection between Input Channel 6 and Output Channels 1 through 4.

Position M can only be programmed when Bank Select = 0.

3.2.2.14 Programming Position N

If Bank Select is 0, position N programs the connection between Input Channel 6 and Output Channels 5 through 8.

Position N can only be programmed when Bank Select = 0.

3.2.2.15 Programming Position O

If Bank Select is 0, the value in position O determines whether Output Channels 1 through 4 are terminated or not.

Position O can only be programmed when Bank Select = 0.

3.2.2.16 Programming Position P

If Bank Select is 0, the value of position P determines whether Output Channels 5 through 8 are terminated or not.

Position P can only be programmed when Bank Select = 0.

3.2.2.17 Reading Card ID

The card ID number can be read back from positions B & C. Since binary number 2^0, 2^1, 2^2, and 2^3 are read back in data position C and binary numbers 2^4, 2^5, 2^6, and 2^7 are read back in data position B, the information in M$ must be converted to a decimal ID number. Since the ASCII characters in each position represent 0 through 15, the result can be treated as a HEX number. In the case of this module, the card ID in HEX and decimal is "04".

Note: The actual characters read back in each data position will be the ASCII characters 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, :, ;, <, =, >, and ? which correspond to the HEX characters 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, and F respectively.

The identification number is read back in the following manner:

1. UTI-1 IEEE-488 bus address = 709, 4 Bit Parallel Bus address = 1, card slot = 5.
2. Send the card select number and the command to interrogate positions B and C ("I" control block for listen operation):

   OUTPUT 709;"W1AA5"&"I1BC"

   The first portion of the output statement, "W1AA5", is a talk operation to select the card slot position of the module (A = 5). The second portion, "I1BC", is a listen operation which interrogates positions B and C of the selected card slot. The output statement can also be written as OUTPUT 709;"W1AA5I1BC".
3. Read back the information from the IEEE-488 bus and assign it to a string variable.

   ENTER 709;Result$

3.2.3 Programming Example

The following example shows how a programming word may be built using the IEEE-488 Bus Interface and HP 200 or 300 series computer. Please refer to the programing sheets.

In the 6 × 8 Balanced Switching Matrix, a control word consists of: "WxS1S2abcdef ghijklmnop"

"x" is the 4 Bit Parallel Bus address for the UTI-1 mainframe

"S_1S_2" are the position selectors; ie. for positions A through J, S_1 = A and S_2 = J.

"a" is the card slot select address

"b" is the bank select (0 or 1)

"c through p" are control data values

Suppose the user had the following configuration requirements:

1) The UTI-1 IEEE-488 bus address = 709, the 4 Bit Parallel Bus address = 1, and the card slot select address = 5. The output statement thus far is:

   OUTPUT 709;"W1AA5"

2) Connect Input Channel 1 to Output Channel 1 (B = 0, C = 1, D = 0). The output statement thus far is:

   OUTPUT 709;"W1AD5010"

3) Connect Input Channel 3 to Output Channel 8 (B = 0, G = 0, H = 8,). The output statement thus far is:

   OUTPUT 709;"W1AD5010"&"GH08"

4) Input Channels 2, 4, 5, and 6 disconnected (E = F = I = J = K = L = M = N = 0). The output statement thus far is:

   OUTPUT 709;"W1AN50100008000000"

5) Terminate all unused Output Channels.

   O = 2 + 4 + 8 = 14 [Terminate CH2 OUT, CH3 OUT, CH4 OUT]*

   P = 1 + 2 + 4 = 7 [Terminate CH5 OUT, CH6 OUT, CH7 OUT]

   The complete output statement is:

   OUTPUT 709;"W1AP50100008000000>7"

6) Connect Input Channel 1 and Input Channel 3 to Matrix (B = 1, and C = 1 + 4 = 5, and D = 0). A second output statement is required and it should be as follows:

   OUTPUT 709;"W1AD5150"

***Note:** Character O = 14, but the ascii character used in the AUX Bus equivalent to 14 is ">".

3.3. Circuit Description

3.3.1 4 Bit Parallel Bus

The CARD SEL (card select) and TALK/LISTEN input signals are combined in IC 4 and IC 1. The TALK/LISTEN input controls whether the low card select pulses are enabling the talk or listen circuitry. When in the talk mode, a low is at St2 pin 45A. This causes the enabling card select pulses to be at IC 4 pin 6. When in the listen mode, a high is at St2 pin 45A. This causes the enabling card select pulses to be at IC 4 pin 3.

In the talk circuitry, two banks control the circuitry. These banks are controlled by program position B. When in position B, a low is felt at IC 5 pin 2 and IC 15 pin 6; in all other positions these points are high. When pin 4 of IC 15 ($\overline{GL}$) is low, this IC acts like a decoder/demultiplexer, but the outputs of the IC are forced high by the low at IC 15 pin 6 (G1). The data in position B is latched when a low to high transition is felt at IC 15 pin 4 ($\overline{GL}$), and this information cannot change as long as IC 15 pin 4 is high. The outputs of this IC are turned on during the low card select pulses and as long as pin 6 (G1) is high; pin 6 will remain high during all program positions other than position B. When position B is programmed to 0, low pulses will be at IC 15 pin 15, causing the activation of the bank 0 circuitry. When position B is programmed to 1, low pulses will be at IC 15 pin 14, causing the activation of bank 1 circuitry. Remember that these pulses will only be at the output pins when positions other than B are being programmed; when B is being programmed, these outputs are forced high.

In bank 0, program positions A through P are written to. This is accomplished by using the POS 2^3 input to switch between two sets of latches. When programming positions C through H, low pulses will be present at IC 3 pin 3, and when programming positions I through P, low pulses will be present at IC 3 pin 6. The pulses at IC 3 pin 3 will cause latch ICs 16 through 19 to be activated, and the pulses at IC 3 pin 6 will cause latch ICs 20 through 23 to be activated. ICs 16 and 20 latch the TALK 2^0 data, ICs 17 and 21 latch the TALK 2^1 data, ICs 18 and 22 latch the TALK 2^2 data, and ICs 19 and 23 latch the TALK 2^3 data.

In bank 1, only program positions C through H can be written to, and only positions C and D are required. When programming positions C through H, low pulses will be at IC 3 pin 8. These pulses activate latch ICs 24 through 27. If positions I through P are written to in bank 1, the high at IC 3 pin 9 will block the enabling pulses. IC 24 latches the TALK 2^0 data, IC 25 latches the TALK 2^1 data, IC 26 latches the TALK 2^2 data, and IC 27 latches the TALK 2^3 data.

When in the listen mode, the low pulses at IC 4 pin 3 enable IC 28. Pin 14 of this IC pulses when interrogating position B, and pin 13 pulses when interrogating position C. These pulses enable IC 29. When interrogating position B, pins 11, 13, 15, and 17 of IC 29 are latched to the listen ports, and when interrogating position C, pins 2, 4, 6, and 8 of IC 29 are latched to the listen ports. The computer will read this information back as a 0 in position B and a 4 in position C. This information corresponds to the card identification number 04.

3.3.2 Relay Drivers

Each Relay is driven by a ULN 2903 inverter. Each of these ICs contains 8 different inverters. A low at the output of each inverter will energize the relay. The input of these ICs is connected to one of the addressable latches.

3.3.3 Relay Matrix

Relays 57 through 62 connect input channels 1 through 6 to the 6 × 8 switching matrix.

Relays 1 through 8 enable the connection of input channel one to any of the eight output channels.

Relays 9 through 16 enable the connection of input channel two to any of the eight output channels.

Relays 17 through 24 enable the connection of input channel three to any of the eight output channels.

Relays 25 through 32 enable the connection of input channel four to any of the eight output channels.

Relays 33 through 40 enable the connection of input channel five to any of the eight output channels.

Relays 41 through 48 enable the connection of input channel six to any of the eight output channels.

Relays 49 through 56 enable the termination of any of the eight output channels.

3 17,18 21 1 25 24 4

2,7,9,10

53

5

6

52 NOTE 2 23 26 23

SEE DETAIL "A"

Bu1

REL 41 REL 33 REL 25 REL 17 REL 9 REL 1 REL 49
REL 42 REL 34 REL 26 REL 18 REL 10 REL 2 REL 50
REL 43 REL 35 REL 27 REL 19 REL 11 REL 3 REL 51
REL 44 REL 36 REL 28 REL 20 REL 12 REL 4 REL 52
REL 62 REL 61 REL 60 REL 59 REL 58 REL 57
REL 45 REL 37 REL 29 REL 21 REL 13 REL 5 REL 53
REL 46 REL 38 REL 30 REL 22 REL 14 REL 6 REL 54
REL 47 REL 39 REL 31 REL 23 REL 15 REL 7 REL 55
REL 48 REL 40 REL 32 REL 24 REL 16 REL 8 REL 56

R11 R10 R13 R12 R15 R14 R17 R16 R19 R18 R21 R20 R23 R22 R25 R24

C14 C22 or R26 C15 C23 or R27 C16 C24 or R28 C17 C25 or R29 C18 C26 or R30 C19 C27 or R31 C20 C28 or R32 C21 C29 or R33

R2 R3 R4 R5 R6 R7 R8 R9

1 64 32 95

L1 C13 R1 C12

1A 50A ST 1 ST 2

IC14 IC16 IC7 IC17 IC24 IC8 IC18 IC25 IC9 IC19 IC26 IC10 IC20 IC27 IC11 IC21 IC12 IC22 IC28 IC13 IC23 IC15 IC4 IC2 IC5 IC1 IC29 IC3

C1 C11 C10 C9 C8 C7 C6 C5 C4 C2 C3

DETAIL "A"

PINS 33 TO 63 ARE FOR FUTURE USE AND ARE NOT AVAILABLE IN THIS SERIES ACTUAL BU1 CONN IS MARKED PINS 1 THRU 64. DETAIL DWG SHOWS PROPER PIN #'S AND LOCATION

1 2 3 64 65 66 30 31 32 93 94 95

NOTES

1) [ ] SOLDERMASK THESE AREAS USING ITEMS 50 & 51
2) R26 THRU R33, OR C22 THRU C29 CAN BE ADDED IN THESE POSITIONS DEPENDING ON CUSTOMER TERMINATION REQUIREMENTS

Oberfläche

Freimaßtoleranzen: WN 51/3/1

Halbzeug und Werkstoffe

Ausgabe	Änderung	Tag	Name
5	88-059	13.4.88	LG
4	87-179	27-11-87	Lars B
3	87-064	24.8.87	LARS B
2	87-034	6.4.87	Lars B
1	———	20-3-87	RAY H

	Tag	Name
Bearb	19-2-87	RAY HENDRICKS
Gepr.	27-3-87	Sanjay "D"
Norm.		

Wandel u Gottermann Reutlingen

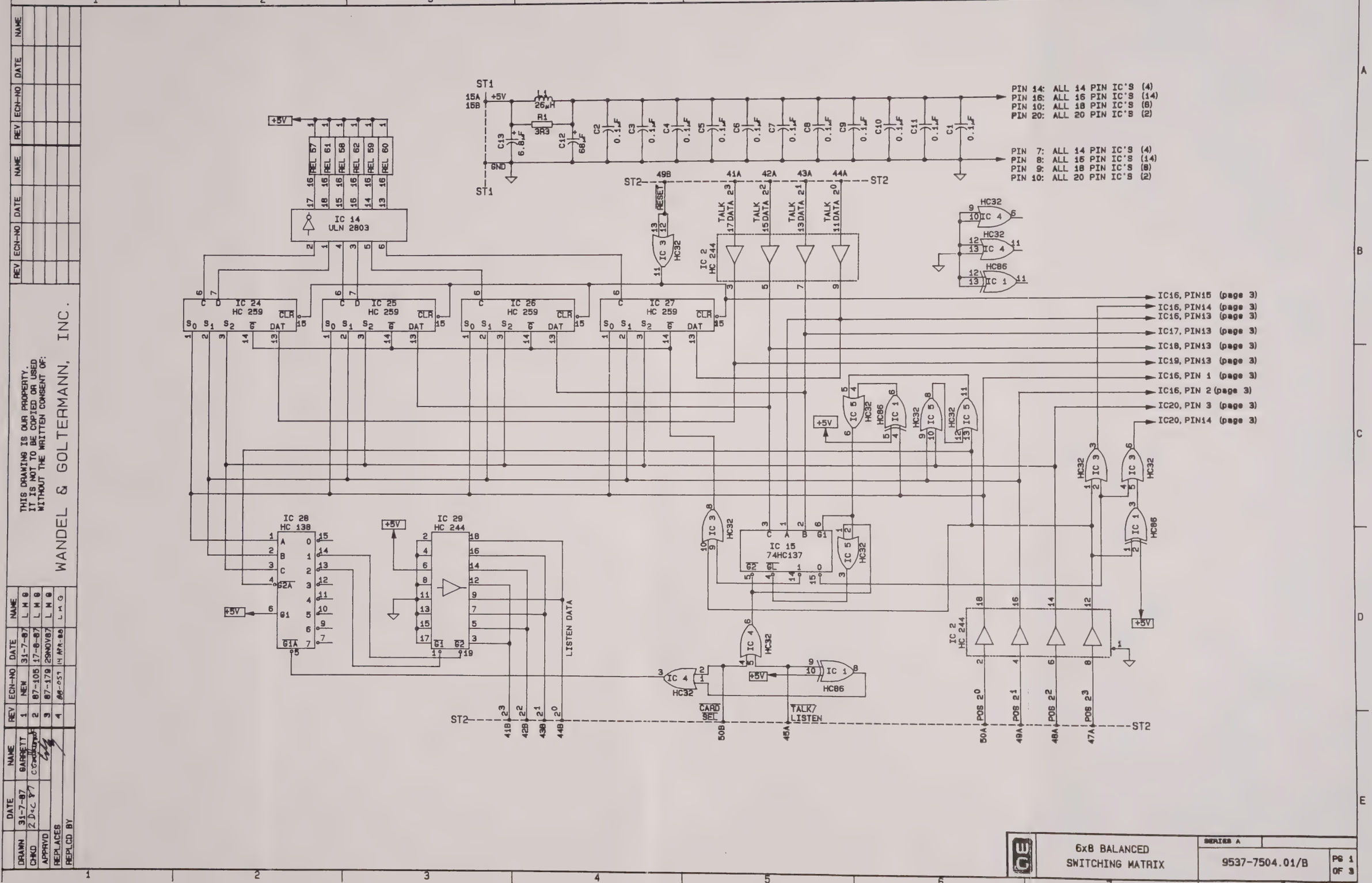
Benennung: 6x8 BALANCED SWITCHING MATRIX (ASSEMBLED)

Maßstab 1/1

9537-7004.00 /34

Ersatz für: Ersatz. Verwdg

SoftRevision 1A5-9



THIS DRAWING IS OUR PROPERTY.
IT IS NOT TO BE COPIED OR USED
WITHOUT THE WRITTEN CONSENT OF:

WANDEL & GOLTERMANN, INC.

	NAME	DATE
DRAWN	GARRETT	31-7-87
CHKD		
APPRVD		
REPLACES		
REPLCD BY		

REV	ECN-NO	DATE	NAME
1	NEW	31-7-87	L M G
2	87-105	17-8-87	L M G
3	87-179	29NOV87	L M G
4	88-051	14 APR 88	L M G

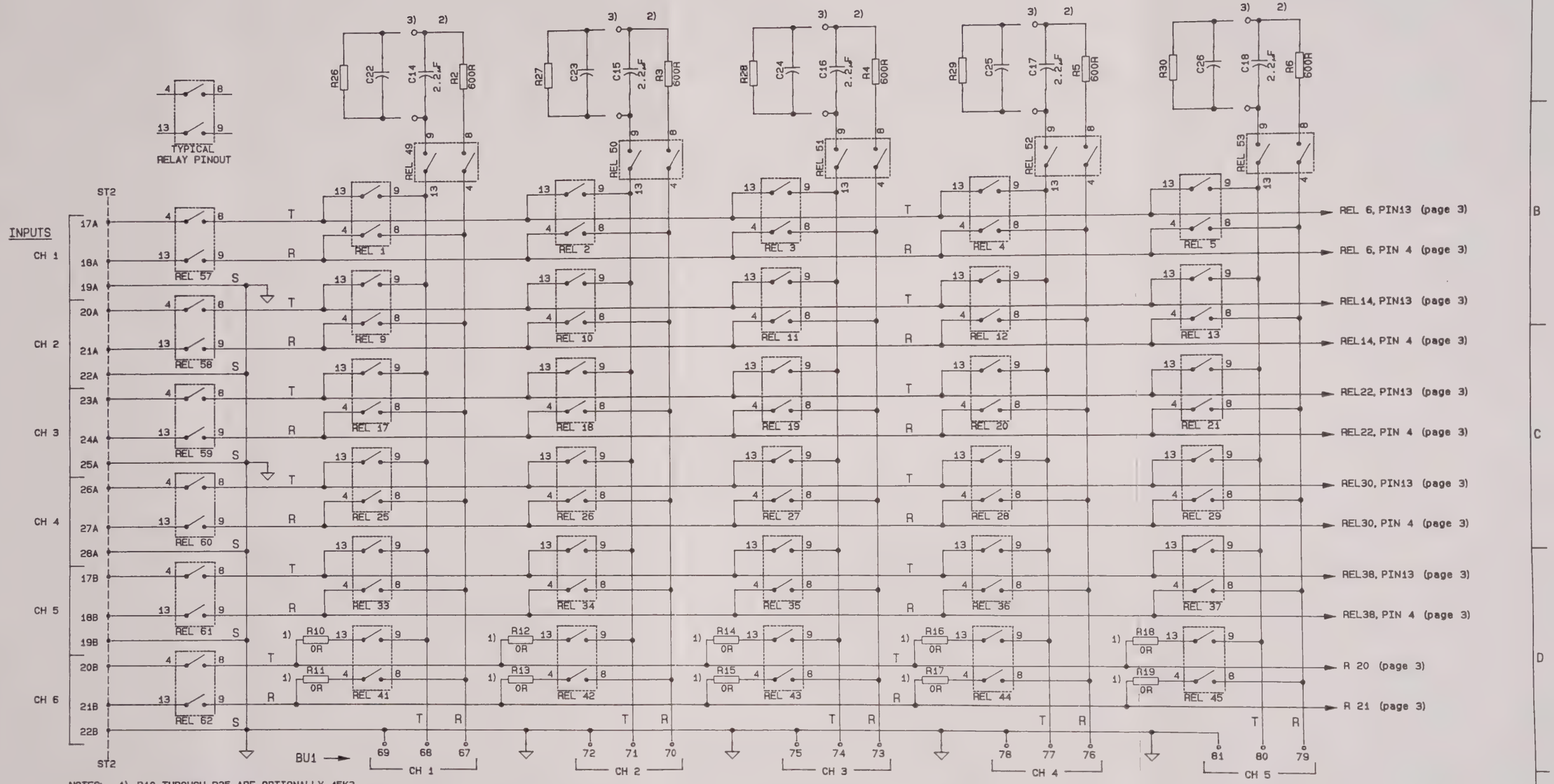
REV	ECN-NO	DATE	NAME

6x8 BALANCED SWITCHING MATRIX

SERIES A

9537-7504.01/B

PG 1 OF 3



NOTES:
1) R10 THROUGH R25 ARE OPTIONALLY 45K3.
2) C14 THROUGH C21, AND R2 THROUGH R9 ARE TERMINATION COMPONENTS. STANDARD VALUES ARE SHOWN. THESE VALUES COULD BE CHANGED TO MATCH CUSTOMER REQUIREMENTS.
3) R26 THROUGH R33 OR C22 THROUGH C29 CAN BE ADDED IN THESE POSITIONS DEPENDING ON CUSTOMER TERMINATION REQUIREMENTS.
4) FOR FUTURE USE BU1 PINS 33 THRU 63 NOT AVAILABLE IN THIS SERIES.

T - TIP
R - RING
S - SLEEVE

REV	ECN-NO	DATE	NAME
1	NEW	30-7-87	L M G
2	87-105	17-8-87	L M G
3	87-179	29NOV87	L M G
4	88-059	14-4-88	L M G

	DATE	NAME
DRAWN	30-7-87	GARRETT
CHKD	10 Apr 88	C Morse
APPRVD		
REPLACES		
REPLCD BY		

THIS DRAWING IS OUR PROPERTY. IT IS NOT TO BE COPIED OR USED WITHOUT THE WRITTEN CONSENT OF:

WANDEL & GOLTERMANN, INC.

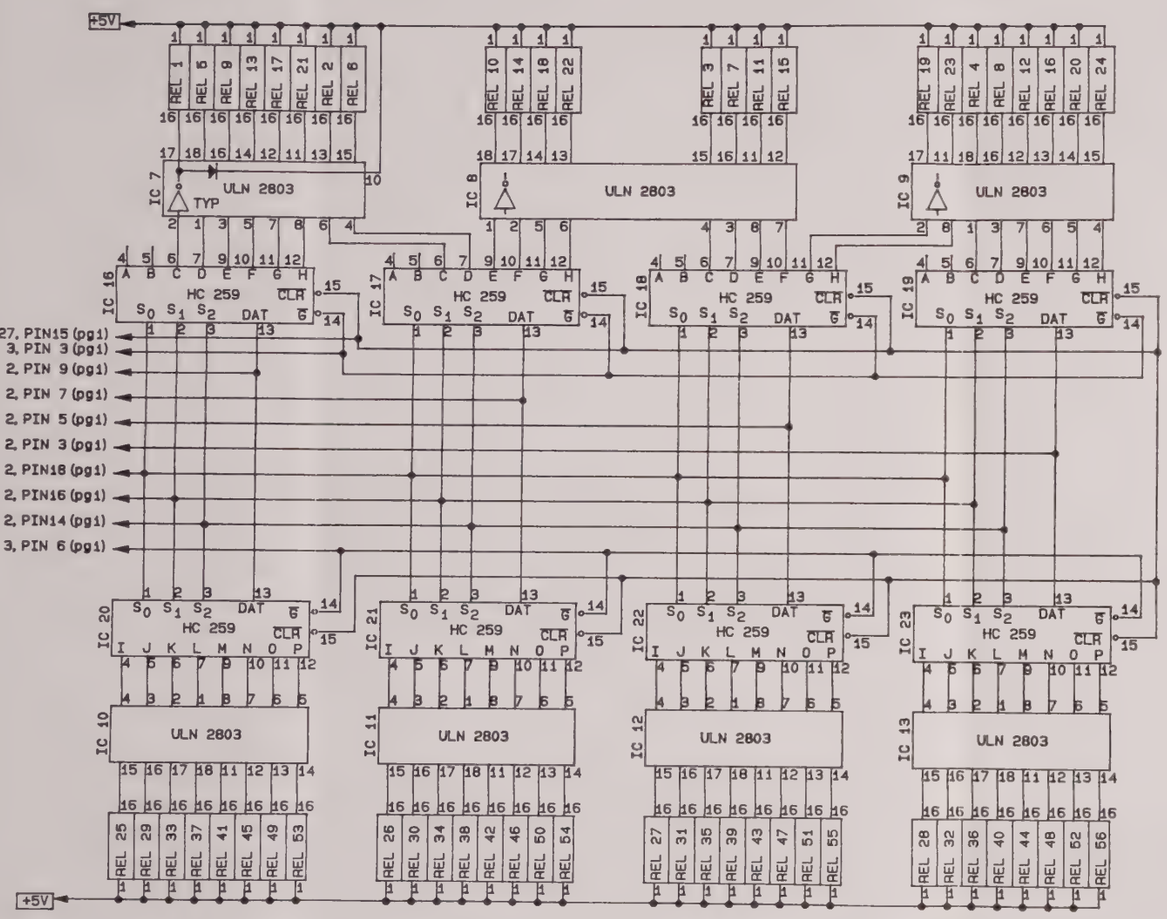
	NAME	DATE	ECN-NO	REV

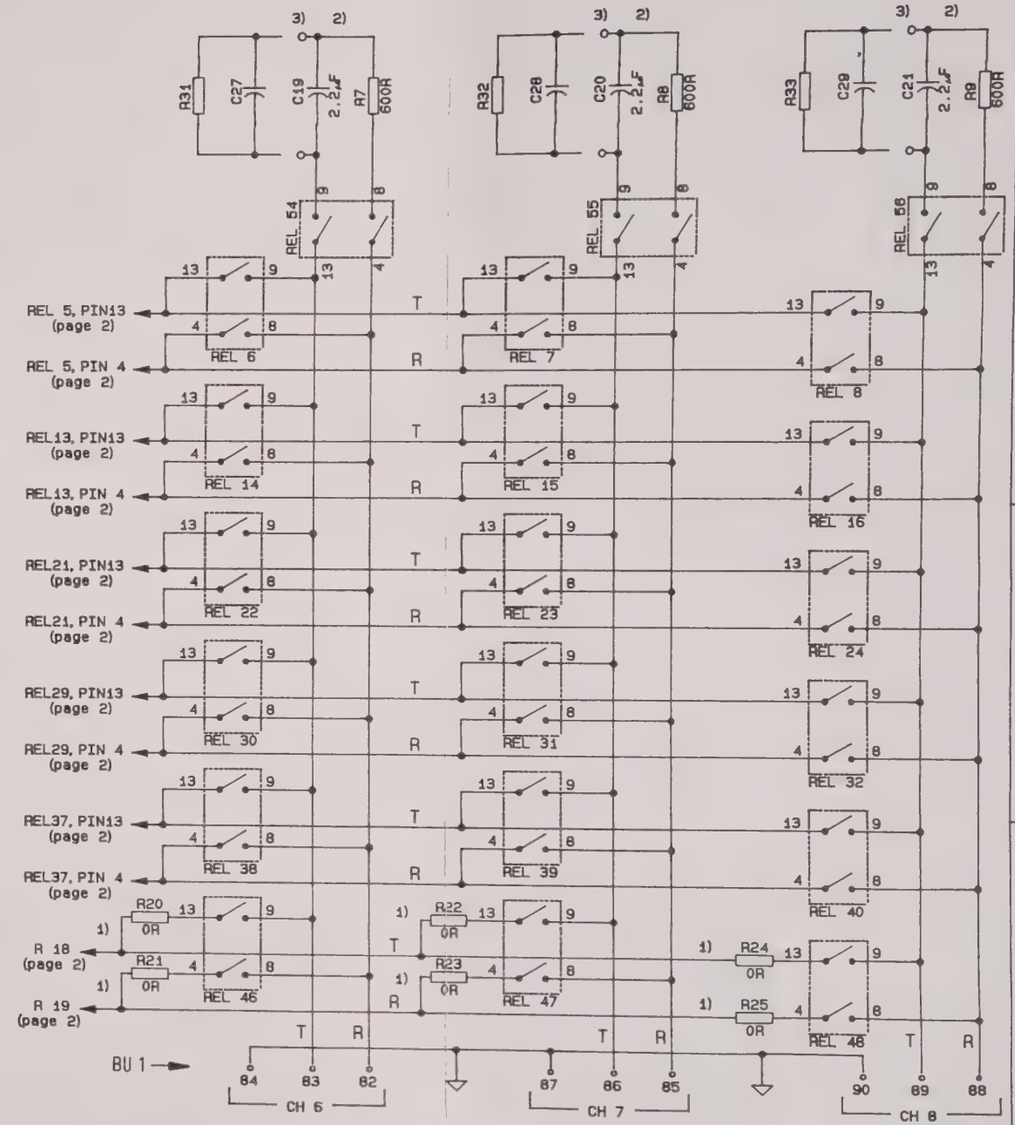
6x8 BALANCED SWITCHING MATRIX

SERIES A...

9537-7504.01/B

PG 2 OF 3





OUTPUTS TO U.U.T.

GROUND INFO:

FOR SERIES D...

- ST1 GND POINTS: 19A, 19B, 24A, 26A, 27B, 32A, 37B, 41B, 42A, 43B, 44A, 45B, 46A, 47B, 48A, 49B
- ST2 GND POINTS: 8A, 9B, 14A

FOR SERIES A THRU C; EXCEPT WITH MODIFICATION 2528: ADDITIONAL GROUNDS ARE:

- ST1 GND POINTS: 20A, 21B, 22A, 23B, 25B, 28A, 29B, 30A, 31B, 33B, 34A, 35B, 36A, 38A, 39B, 40A, 50A
- ST2 GND POINTS: 1B, 2A, 3B, 4A, 5B, 6A, 7B, 10A, 11B, 12A, 13B

NOTES:
1) R10 THROUGH R25 ARE OPTIONALLY 45K3.
2) C14 THROUGH C21, AND R2 THROUGH R9 ARE TERMINATION COMPONENTS. STANDARD VALUES ARE SHOWN. THESE VALUES COULD BE CHANGED TO MATCH CUSTOMER REQUIREMENTS.
3) R26 THROUGH R33 OR C22 THROUGH C29 CAN BE ADDED IN THESE POSITIONS DEPENDING ON CUSTOMER TERMINATION REQUIREMENTS.
4) FOR FUTURE USE. BU1 PINS 33 THRU 63 NOT AVAILABLE IN THIS SERIES.

THIS DRAWING IS OUR PROPERTY.
IT IS NOT TO BE COPIED OR USED
WITHOUT THE WRITTEN CONSENT OF:
WANDEL & GOLTERMANN, INC.

REV	ECN-NO	DATE	NAME
1	NEW	30-7-87	L M G
2	87-105	17-8-87	L M G
3	87-179	29NOV87	L M G
4	88-059	14APR88	L M G

	NAME	DATE
DRAWN	BARRETT	30-7-87
CHKD		20 Apr 88
APPRVD		
REPLACES		
REPLCD BY		

6x8 BALANCED SWITCHING MATRIX

SERIES A...

9537-7504.01/B

PG 3 OF 3

WANDEL & GOLTERMANN TECHNOLOGIES, INC.

6x8 BALANCED SWITCHING MODULE

BN 9537 ********** LIST OF REPLACEABLE PARTS ********** SERIES: ALL DATE: Jan 8, 1990

DIAG	REF	ITEM	QTY	PART NUMBER	DESCRIPTION	STOCK LOCATION	VERS/OPT	SERIES STRT	SERIES END	SUBASSEMBLY 9537-XXXX	SUBASSEMBLY CODE
							00 04			7004	S
		0	0	9537-7004.003	6X8 SWITCHING MATRIX		00 04			7004	A
		1	1	9537-7004.029	PC BOARD MACHINED		00 04			7004	
		3	1	9537-7004.053	PANEL REAR MARKED		00 04			7004	M
		5	1	0000-2911.029	LABEL SERIAL ABC		00 04			7004	
		6	1	9537-7001.064	BLOCK PANEL MTG 1		00 04			7004	
		7	2	9537-7001.080	BLOCK PANEL MTG 2		00 04			7004	
		21	32		RECEPT PIN ANG ROW#3	XX03-0518.00	00 04			7004	
		23	4	0000-7518.308	SOCKET IC DIP 14		00 04			7004	
		24	14	0000-7518.391	SOCKET IC 16 PIN DIP		00 04			7004	
		25	8	0000-7675.386	SOCKET IC DIP 18 .3"		00 04			7004	
		26	2	0000-7584.590	SOCKET IC DIP 20		00 04			7004	
		53	1	0001-0072.460	LABEL YEL/BLK C-MOS		00 04			7004	
4	BU	1	1	9537-0000.101	CONN MODIFIED 64P		00 04			7004	M
4	C	1	1	0000-7632.659	C-CER 100N 10% 50V		00 04			7004	
4	C	2	1	0000-7632.659	C-CER 100N 10% 50V		00 04			7004	
4	C	3	1	0000-7632.659	C-CER 100N 10% 50V		00 04			7004	
4	C	4	1	0000-7632.659	C-CER 100N 10% 50V		00 04			7004	
4	C	5	1	0000-7632.659	C-CER 100N 10% 50V		00 04			7004	
4	C	6	1	0000-7632.659	C-CER 100N 10% 50V		00 04			7004	
4	C	7	1	0000-7632.659	C-CER 100N 10% 50V		00 04			7004	
4	C	8	1	0000-7632.659	C-CER 100N 10% 50V		00 04			7004	
4	C	9	1	0000-7632.659	C-CER 100N 10% 50V		00 04			7004	
4	C	10	1	0000-7632.659	C-CER 100N 10% 50V		00 04			7004	
4	C	11	1	0000-7632.659	C-CER 100N 10% 50V		00 04			7004	
4	C	12	1		CAP TANT 68uF 6V	XX32-0005.00	00 04			7004	
4	C	13	1		C-ELYT TA 6.8U10%35V	XX32-0006.00	00 04			7004	
4	C	14	1	0001-0010.556	C-MKT 2.2u 10% 100V		00 04			7004	
4	C	15	1	0001-0010.556	C-MKT 2.2u 10% 100V		00 04			7004	
4	C	16	1	0001-0010.556	C-MKT 2.2u 10% 100V		00 04			7004	
4	C	17	1	0001-0010.556	C-MKT 2.2u 10% 100V		00 04			7004	
4	C	18	1	0001-0010.556	C-MKT 2.2u 10% 100V		00 04			7004	
4	C	19	1	0001-0010.556	C-MKT 2.2u 10% 100V		00 04			7004	
4	C	20	1	0001-0010.556	C-MKT 2.2u 10% 100V		00 04			7004	
4	C	21	1	0001-0010.556	C-MKT 2.2u 10% 100V		00 04			7004	
4	C	22	0				00 04			7004	

DIAG	REF	ITEM	QTY	PART NUMBER	DESCRIPTION	STOCK LOCATION	VERS/OPT	SERIES STRT	SERIES END	SUBASSEMBLY 9537-XXXX	CODE
4	C	23	0				00	04			7004
4	C	24	0				00	04			7004
4	C	25	0				00	04			7004
4	C	26	0				00	04			7004
4	C	27	0				00	04			7004
4	C	28	0				00	04			7004
4	C	29	0				00	04			7004
4	IC	1	1	0000-7597.244	IC MOS 74HC86	D14	00	04			7004
4	IC	2	1	0000-7594.959	IC MOS 74HC244	D20	00	04			7004
4	IC	3	1	0000-7597.176	IC MOS 74HC32	D14	00	04			7004
4	IC	4	1	0000-7597.176	IC MOS 74HC32	D14	00	04			7004
4	IC	5	1	0000-7597.176	IC MOS 74HC32	D14	00	04			7004
4	IC	7	1	0000-7579.657	IC DRVR ULN2803A	D18	00	04			7004
4	IC	8	1	0000-7579.657	IC DRVR ULN2803A	D18	00	04			7004
4	IC	9	1	0000-7579.657	IC DRVR ULN2803A	D18	00	04			7004
4	IC	10	1	0000-7579.657	IC DRVR ULN2803A	D18	00	04			7004
4	IC	11	1	0000-7579.657	IC DRVR ULN2803A	D18	00	04			7004
4	IC	12	1	0000-7579.657	IC DRVR ULN2803A	D18	00	04			7004
4	IC	13	1	0000-7579.657	IC DRVR ULN2803A	D18	00	04			7004
4	IC	14	1	0000-7579.657	IC DRVR ULN2803A	D18	00	04			7004
4	IC	15	1	0000-7607.163	IC MOS 74HC137	D16	00	04			7004
4	IC	16	1	0000-7597.590	IC MOS 74HC259	D16	00	04			7004
4	IC	17	1	0000-7597.590	IC MOS 74HC259	D16	00	04			7004
4	IC	18	1	0000-7597.590	IC MOS 74HC259	D16	00	04			7004
4	IC	19	1	0000-7597.590	IC MOS 74HC259	D16	00	04			7004
4	IC	20	1	0000-7597.590	IC MOS 74HC259	D16	00	04			7004
4	IC	21	1	0000-7597.590	IC MOS 74HC259	D16	00	04			7004
4	IC	22	1	0000-7597.590	IC MOS 74HC259	D16	00	04			7004
4	IC	23	1	0000-7597.590	IC MOS 74HC259	D16	00	04			7004
4	IC	24	1	0000-7597.590	IC MOS 74HC259	D16	00	04			7004
4	IC	25	1	0000-7597.590	IC MOS 74HC259	D16	00	04			7004
4	IC	26	1	0000-7597.590	IC MOS 74HC259	D16	00	04			7004
4	IC	27	1	0000-7597.590	IC MOS 74HC259	D16	00	04			7004
4	IC	28	1	0000-7597.309	IC MOS 74HC138	D16	00	04			7004
4	IC	29	1	0000-7594.959	IC MOS 74HC244	D20	00	04			7004
4	L	1	1	0001-0042.757	L-FERRITE 27U HORIZ		00	04			7004

WANDEL & GOLTERMANN TECHNOLOGIES, INC.

6x8 BALANCED SWITCHING MODULE

BN 9537 ********** LIST OF REPLACEABLE PARTS ********** SERIES: ALL DATE: Jan 8, 1990

DIAG	REF	ITEM	QTY	PART NUMBER	DESCRIPTION	STOCK LOCATION	VERS/OPT	SERIES STRT	SERIES END	SUBASSEMBLY 9537-XXXX	CODE
4	R	1	1	0000-7629.743	R-MF 3.32R 2% 204		00 04				7004
4	R	2	1		R-WW 600R 1% NI 3W	XX08-0838.00	00 04				7004
4	R	3	1		R-WW 600R 1% NI 3W	XX08-0838.00	00 04				7004
4	R	4	1		R-WW 600R 1% NI 3W	XX08-0838.00	00 04				7004
4	R	5	1		R-WW 600R 1% NI 3W	XX08-0838.00	00 04				7004
4	R	6	1		R-WW 600R 1% NI 3W	XX08-0838.00	00 04				7004
4	R	7	1		R-WW 600R 1% NI 3W	XX08-0838.00	00 04				7004
4	R	8	1		R-WW 600R 1% NI 3W	XX08-0838.00	00 04				7004
4	R	9	1		R-WW 600R 1% NI 3W	XX08-0838.00	00 04				7004
4	R	10	1	0000-7555.228	R-MF 0 OHM JUMP 207		00 04				7004
4	R	11	1	0000-7555.228	R-MF 0 OHM JUMP 207		00 04				7004
4	R	12	1	0000-7555.228	R-MF 0 OHM JUMP 207		00 04				7004
4	R	13	1	0000-7555.228	R-MF 0 OHM JUMP 207		00 04				7004
4	R	14	1	0000-7555.228	R-MF 0 OHM JUMP 207		00 04				7004
4	R	15	1	0000-7555.228	R-MF 0 OHM JUMP 207		00 04				7004
4	R	16	1	0000-7555.228	R-MF 0 OHM JUMP 207		00 04				7004
4	R	17	1	0000-7555.228	R-MF 0 OHM JUMP 207		00 04				7004
4	R	18	1	0000-7555.228	R-MF 0 OHM JUMP 207		00 04				7004
4	R	19	1	0000-7555.228	R-MF 0 OHM JUMP 207		00 04				7004
4	R	20	1	0000-7555.228	R-MF 0 OHM JUMP 207		00 04				7004
4	R	21	1	0000-7555.228	R-MF 0 OHM JUMP 207		00 04				7004
4	R	22	1	0000-7555.228	R-MF 0 OHM JUMP 207		00 04				7004
4	R	23	1	0000-7555.228	R-MF 0 OHM JUMP 207		00 04				7004
4	R	24	1	0000-7555.228	R-MF 0 OHM JUMP 207		00 04				7004
4	R	25	1	0000-7555.228	R-MF 0 OHM JUMP 207		00 04				7004
4	R	26	0				00 04				7004
4	R	27	0				00 04				7004
4	R	28	0				00 04				7004
4	R	29	0				00 04				7004
4	R	30	0				00 04				7004
4	R	31	0				00 04				7004
4	R	32	0				00 04				7004
4	R	33	0				00 04				7004
4	REL	1	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 04				7004
4	REL	2	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 04				7004
4	REL	3	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 04				7004

WANDEL & GOLTERMANN TECHNOLOGIES, INC.

6x8 BALANCED SWITCHING MODULE

BN 9537 ********** LIST OF REPLACEABLE PARTS ********** SERIES: ALL DATE: Jan 8, 1990

DIAG	REF	ITEM	QTY	PART NUMBER	DESCRIPTION	STOCK LOCATION	VERS/OPT	SERIES STRT	SERIES END	SUBASSEMBLY 9537-XXXX	SUBASSEMBLY CODE
4	REL	4	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 04				7004
4	REL	5	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 04				7004
4	REL	6	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 04				7004
4	REL	7	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 04				7004
4	REL	8	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 04				7004
4	REL	9	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 04				7004
4	REL	10	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 04				7004
4	REL	11	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 04				7004
4	REL	12	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 04				7004
4	REL	13	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 04				7004
4	REL	14	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 04				7004
4	REL	15	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 04				7004
4	REL	16	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 04				7004
4	REL	17	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 04				7004
4	REL	18	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 04				7004
4	REL	19	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 04				7004
4	REL	20	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 04				7004
4	REL	21	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 04				7004
4	REL	22	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 04				7004
4	REL	23	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 04				7004
4	REL	24	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 04				7004
4	REL	25	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 04				7004
4	REL	26	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 04				7004
4	REL	27	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 04				7004
4	REL	28	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 04				7004
4	REL	29	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 04				7004
4	REL	30	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 04				7004
4	REL	31	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 04				7004
4	REL	32	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 04				7004
4	REL	33	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 04				7004
4	REL	34	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 04				7004
4	REL	35	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 04				7004
4	REL	36	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 04				7004
4	REL	37	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 04				7004
4	REL	38	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 04				7004
4	REL	39	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 04				7004

WANDEL & GOLTERMANN TECHNOLOGIES, INC.

6x8 BALANCED SWITCHING MODULE

BN 9537 ********** LIST OF REPLACEABLE PARTS ********** SERIES: ALL

DATE: Jan 8, 1990

DIAG	REF	ITEM	QTY	PART NUMBER	DESCRIPTION	STOCK LOCATION	VERS/OPT	SERIES STRT	SERIES END	SUBASSEMBLY 9537-XXXX	CODE
4	REL	40	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 04				7004
4	REL	41	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 04				7004
4	REL	42	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 04				7004
4	REL	43	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 04				7004
4	REL	44	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 04				7004
4	REL	45	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 04				7004
4	REL	46	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 04				7004
4	REL	47	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 04				7004
4	REL	48	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 04				7004
4	REL	49	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 04				7004
4	REL	50	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 04				7004
4	REL	51	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 04				7004
4	REL	52	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 04				7004
4	REL	53	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 04				7004
4	REL	54	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 04				7004
4	REL	55	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 04				7004
4	REL	56	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 04				7004
4	REL	57	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 04				7004
4	REL	58	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 04				7004
4	REL	59	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 04				7004
4	REL	60	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 04				7004
4	REL	61	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 04				7004
4	REL	62	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 04				7004

Custom Termination Module BN 9537/00.06

Contents **Page**

1. Introduction 1-1
2. Specifications 2-1
   - 2.1. Power Consumption 2-1
   - 2.2. Custom Complex Impedances 2-1
   - 2.3. Programmable Decadic Resistances 2-1
   - 2.4. Relay Characteristics 2-1
3. Operating Description 3-1
   - 3.1. Detailed Description of Features 3-1
     - 3.1.1 Programmable Decadic Resistance 3-2
     - 3.1.2 Custom Complex Impedances 3-2
     - 3.1.3 Programmable Decadic Resistance and Custom Complex Impedance in Series or Parallel 3-3
   - 3.2. Programming 3-5
     - 3.2.1 Programming Sheets 3-5
     - 3.2.2 Programming Description 3-15
       - 3.2.2.1 Programming Position A 3-15
       - 3.2.2.2 Programming Position B 3-15
       - 3.2.2.3 Programming Position C 3-15
       - 3.2.2.4 Programming Position D 3-15
       - 3.2.2.5 Programming Position E 3-15
       - 3.2.2.6 Programming Position F 3-15
       - 3.2.2.7 Programming Position G 3-15
       - 3.2.2.8 Programming Position H 3-16
       - 3.2.2.9 Programming Position I 3-16
       - 3.2.2.10 Programming Position J 3-16
       - 3.2.2.11 Programming Position K 3-16
       - 3.2.2.12 Programming Position L 3-16
       - 3.2.2.13 Programming Position M 3-16
       - 3.2.2.14 Programming Position N 3-16
       - 3.2.2.15 Programming Position O 3-16
       - 3.2.2.16 Programming Position P 3-16
       - 3.2.2.17 Reading Card ID 3-17
     - 3.2.3 Programming Example 3-17
   - 3.3. Circuit Description 3-19
     - 3.3.1 4 Bit Parallel Bus 3-19
     - 3.3.2 Intermediate Bus and Wire Wrap Connections 3-19
     - 3.3.3 Programmable Decadic Resistance 3-19
     - 3.3.4 Custom Complex Impedances 3-20
   - 3.4. Schematic Diagram / Parts List 3-21

Custom Termination Module Description and Operation

1. Introduction

The Custom Termination Module has two internal busses. One bus is connected to a programmable decadic resistance and the other bus can select any combination of 27 complex impedances which can be soldered on the prototype area provided on the board.

The two internal busses can be connected to any of six analog busses running on the UTI-1 motherboard through wire-wrap connections. The standard connection is to Analog Bus 4. They can also be connected to the analog busses coming from the Interchangeable Test Adapter through the front connector by wire wrap connections. The internal busses can be used separately, in series or in parallel combination.

2. Specifications

2.1. Power Consumption

Maximum power consumption per module

1) Power consumption during normal usage. Up to twenty relays are energized. This allows for different combinations of Programmable Decadic Impedances and Complex Impedances.

	+5V	+1V	-15V	Total
Current (Amps)	1.6	-----	-----	-----
Power (Watts)	8.0	-----	-----	8.0

2) Power consumption during minimal usage. Up to twelve relays are energized. This will allow the connection of two complex impedances in series or parallel with a Programmable Decedic Impedance of no more than 6 relays.

	+5V	+1V	-15V	Total
Current (Amps)	1.0	-----	-----	-----
Power (Watts)	5.0	-----	-----	5.0

3) Power consumption with all relays energized. This condition is not typical.

	+5V	+1V	-15V	Total
Current (Amps)	5.0	-----	-----	-----
Power (Watts)	25.0	-----	-----	25.0

2.2. Custom Complex Impedances

Complex Impedance Combinations 27
Prototype Area . . . . . approx. 105 square cm

2.3. Programmable Decadic Resistances

Programmable Decadic Resistances . . . . . 1Ω to 1.666525 MΩ
Programmable Decadic Resistance Accuracy . . . . . ±1%
Programmable Steps 1Ω
Power Rating . . . . . 2 Watts

2.4. Relay Characteristics

Relay contact pull in time . . . . . 3 msec
Relay contact release time . . . . . 2 msec
Relay carrying current . . . . . 3.0 Amps maximum
Relay switching current . . . . . 2.0 Amps maximum
Relay switching voltage . . . . . 250 Volts
Min. expected life under 30 V DC
and 1 Amp load . . . . . 2×10^6 operations

3. Operating Description

3.1. Detailed Description of Features

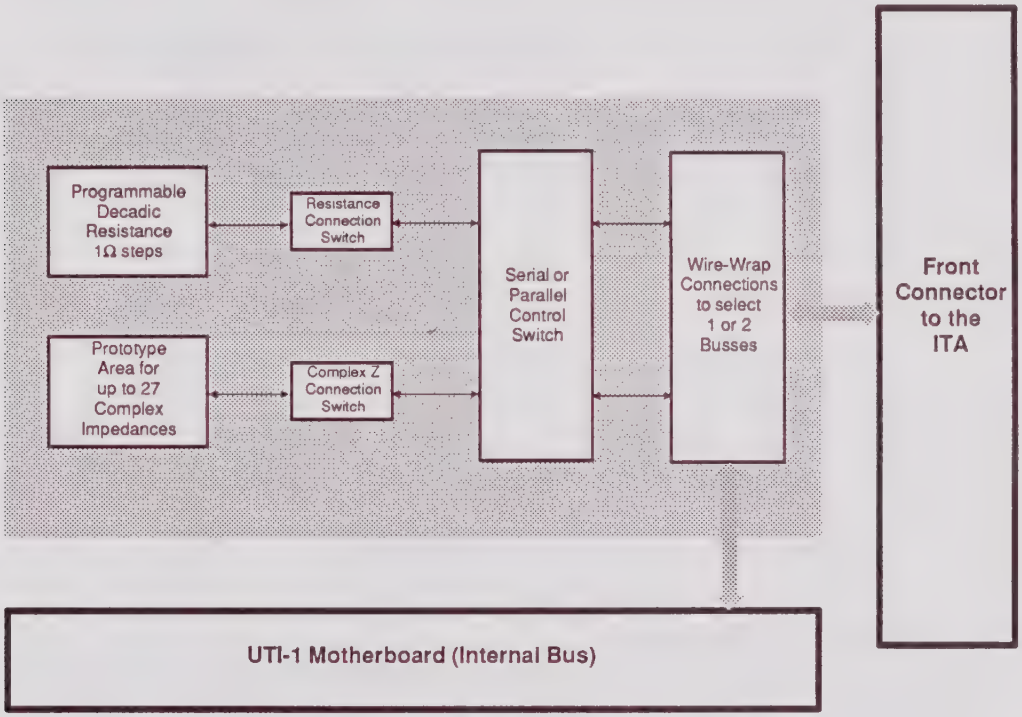


Figure 3.1. Basic Block Diagram

3.1.1 Programmable Decadic Resistance

The programmable decadic section of this module can be set from 1Ω to 1.666525 MΩ in 1Ω steps. There are six different programming steps; these are 1Ω, 10Ω, 100Ω, 1KΩ, 10KΩ, and 100KΩ. Each step can be programmed from 0 to 15. See the programming section and circuit description on how this is accomplished.

Figure 3.1.1 Programmable Decadic Resistances

3.1.2 Custom Complex Impedance

In this section of the circuit, any complex impedance, depending on test requirements, can be installed. There is twenty-seven different relays which can be used to switch in these terminations. There are two types of relay connections; see Figure 3.1.2.

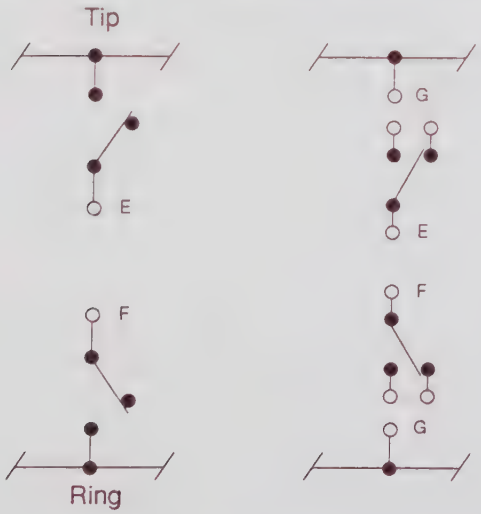


Figure 3.1.2 Custom Termination Relays

3.1.3 Programmable Decadic Resistance and Custom Complex Impedance in Series or Parallel

The programmable decadic resistance can be combined in series or parallel with the custom complex impedance and connected to bus 1.

3.2. Programming

3.2.1 Programming Sheets

Custom Termination Module
9537/00.06

Position	Function	A	B	C	D	E F G H I J K L M N O P	Notes
	Card Select	X					
B	Intermediate Bus Tip conn. to Bus #1 (Rel 1)		1				1
	Intermediate Bus Ring conn. to Bus #1 (Rel 2)		2				
	Intermediate Bus Tip conn. to Ground (Rel 3)		4				
	Intermediate Bus Ring conn. to Ground (Rel 4)		8				
C	Resistance connected to Intermediate Bus (Rel 5)			1			1, 2
	Complex Z connected to Intermediate Bus (Rel 6)			2			
	Complex Z conn. in Ser. w/Intermed. Bus (Rel 7)			4			
	Complex Z connected to Bus #2 (Rel 8)			8			
D	Complex Z enabled (Rel 9)				1		1
	Complex Z, Pins 1E & 1F enabled (Rel 10)				2		
	Complex Z, Pins 2E & 2F enabled (Rel 11)				4		
	Complex Z, Pins 3E & 3F enabled (Rel 12)				8		

Position	Function	A	B C D	E	F	G	H I J K L M N O P	Notes
	Card Select	X						
E	Complex Z, Pins 4E & 4F enabled (Rel 13)			1				
	Complex Z, Pins 5E & 5F enabled (Rel 14)			2				
	Complex Z, Pins 6E & 6F enabled (Rel 15)			4				
	Complex Z, Pins 7E & 7F enabled (Rel 16)			8				
F	Complex Z, Pins 8E & 8F enabled (Rel 17)				1			
	Complex Z, Pins 9E & 9F enabled (Rel 18)				2			
	Complex Z, Pins 10E & 10F enabled (Rel 19)				4			
	Complex Z, Pins 11E & 11F enabled (Rel 20)				8			
G	Complex Z, Pins 12E & 12F enabled (Rel 21)					1		
	Complex Z, Pins 13E & 13F enabled (Rel 22)					2		
	Complex Z, Pins 14E & 14F enabled (Rel 23)					4		
	Complex Z, Pins 15E & 15F enabled (Rel 24)					8		

Position	Function	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Notes
A	Card Select	X																
H	Complex Z, Pins 16E & 16F enabled (Rel 25)								1									
	Complex Z, Pins 17E & 17F enabled (Rel 26)								2									
	Complex Z, Pins 18E & 18F enabled (Rel 27)								4									
	Complex Z, Pins 19E & 19F enabled (Rel 28)								8									
I	Complex Z, Pins 20E & 20F enabled (Rel 29)									1								
	Complex Z, Pins 21E & 21F enabled (Rel 30)									2								
	Complex Z, Pins 22E & 22F enabled (Rel 31)									4								
	Complex Z, Pins 23E & 23F enabled (Rel 32)									8								
J	Complex Z, Pins 24E & 24F enabled (Rel 33)										1							
	Complex Z, Pins 25E & 25F enabled (Rel 34)										2							
	Complex Z, Pins 26E & 26F enabled (Rel 35)										4							
	Complex Z, Pins 26E & 26F enabled (Rel 36)										8							

Position	Function	A	B C D E F G H I J	K	L	M	N O P	Notes
A	Card Select	X						
K	Resistance 10^0 Decade (Rel 37)			1				3
	(Rel 38)			2				
	(Rel 39)			4				
	(Rel 40)			8				
L	Resistance 10^1 Decade (Rel 41)				1			3
	(Rel 42)				2			
	(Rel 43)				4			
	(Rel 44)				8			
M	Resistance 10^2 Decade (Rel 45)					1		3
	(Rel 46)					2		
	(Rel 47)					4		
	(Rel 48)					8		

Position	Function	A	B C D E F G H I J K L M	N	O	P	Notes
A	Card Select	X					
N	Resistance 10^3 Decade (Rel 49)			1			3
	(Rel 50)			2			
	(Rel 51)			4			
	(Rel 52)			8			
O	Resistance 10^4 Decade (Rel 53)				1		3
	(Rel 54)				2		
	(Rel 55)				4		
	(Rel 56)				8		
P	Resistance 10^5 Decade (Rel 57)					1	3
	(Rel 58)					2	
	(Rel 59)					4	
	(Rel 60)					8	

Notes:
1. Add the corresponding bits to get desired combination.
2. When position C4 is programmed ON, C2 and C8 must be programmed OFF.
3. For resistances programmed in BCD or binary, the value is equal to the decade × bit(s) program.

3.2.2 Programming Description

Programming the Custom Termination Module is accomplished through a 4 Bit Parallel Bus. This bus uses "W" control blocks for talk operations and "I" control blocks for listen operations (see 4 Bit Parallel Bus section of this manual).

A complete control block for this module contains sixteen positions (A through P) and each position has sixteen possible values. These values are number 0 through 9 and the ASCII character equivalents of 10, 11, 12, 13, 14, and 15 which are :, ;, <, =, >, and ? respectively.

3.2.2.1 Programming Position A

Position A is used to select the proper card in the UTI-1. The value used in this position corresponds to the slot number in which the Custom Termination Module is located. When looking at the back of the UTI-1, the right most location corresponds to slot number 0 and the left most location corresponds to slot number 15. If you do not program this position, the information will never reach this module.

3.2.2.2 Programming Position B

Position B is used for the intermediate bus connections. Each side of the bus 1 pins can be connected to the intermediate bus separately, and each side of the intermediate bus can be connected to ground. The intermediate bus is the connection between bus 1 and decadic resistances and or complex impedances.

3.2.2.3 Programming Position C

Position C is used to connect the intermediate bus to the decadic resistance and or the complex impedance. The complex impedance can be connected in series or in parallel with the decadic resistance.

3.2.2.4 Programming Position D

Position D is used to enable the entire complex impedance section and to enable the first three complex impedance sections.

3.2.2.5 Programming Position E

Position E is used to enable the fourth, fifth, sixth, and seventh complex impedances.

3.2.2.6 Programming Position F

Position F is used to enable the eighth, ninth, tenth, and eleventh complex impedances.

3.2.2.7 Programming Position G

Position G is used to enable the twelfth, thirteenth, fourteenth, and fifteenth complex impedances.

3.2.2.8 Programming Position H

Position H is used to enable the sixteenth, seventeenth, eighteenth, and nineteenth complex impedances.

3.2.2.9 Programming Position I

Position I is used to enable the twentieth, twenty-first, twenty-second, and twenty-third complex impedances.

3.2.2.10 Programming Position J

Position J is used to enable the twenty-fourth, twenty-fifth, twenty-sixth, and twenty-seventh complex impedances.

3.2.2.11 Programming Position K

Position K is used to program the decadic programmable resistances in 1Ω steps. The steps can be programmed from 0Ω to 15Ω. Enter the amount of impedance required. For 10, 11, 12, 13, 14, and 15, enter :, ;, <, =, >, and ? respectively.

3.2.2.12 Programming Position L

Position L is used to program the decadic programmable resistances in 10Ω steps. The steps can be programmed from 0Ω to 150Ω. Enter the amount of 10Ω steps required; for 10, 11, 12, 13, 14, and 15, enter :, ;, <, =, >, and ? respectively. Example: for 90Ω, enter 9.

3.2.2.13 Programming Position M

Position M is used to program the decadic programmable resistances in 100Ω steps. The steps can be programmed from 0Ω to 1500Ω. Enter the amount of 100Ω steps required; for 10, 11, 12, 13, 14, and 15, enter :, ;, <, =, >, and ? respectively. Example: for 900Ω, enter 9.

3.2.2.14 Programming Position N

Position N is used to program the decadic programmable resistances in 1KΩ steps. The steps can be programmed from 0Ω to 15KΩ. Enter the amount of 1KΩ steps required; for 10, 11, 12, 13, 14, and 15, enter :, ;, <, =, >, and ? respectively. Example: for 9KΩ, enter 9.

3.2.2.15 Programming Position O

Position O is used to program the decadic programmable resistances in 10KΩ steps. The steps can be programmed from 0Ω to 150KΩ. Enter the amount of 10KΩ steps required; for 10, 11, 12, 13, 14, and 15, enter :, ;, <, =, >, and ? respectively. Example: for 90KΩ, enter 9.

3.2.2.16 Programming Position P

Position P is used to program the decadic programmable resistances in 100KΩ steps. The steps can be programmed from 0Ω to 1500KΩ. Enter the amount of 100KΩ steps required; for 10, 11, 12, 13, 14, and 15, enter :, ;, <, =, >, and ? respectively. Example: for 900KΩ, enter 9.

3.2.2.17 Reading Card ID

The card ID number can be read back from positions B & C. Since binary number 2^0, 2^1, 2^2, and 2^3 are read back in data position C and binary numbers 2^4, 2^5, 2^6, and 2^7 are read back in data position B, the information in M$ must be converted to a decimal ID number. Since the ASCII characters in each position represent 0 through 15, the result can be treated as a HEX number. In case of this module, the card ID in HEX and decimal is "06".

Note: The actual characters read back in each data position will be the ASCII characters 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, :, ;, <, =, >, and ? which correspond to the HEX characters 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, and F respectively.

Th identification number is read back in the following manner:

1. UTI-1 IEEE-488 bus address = 709, 4 Bit Parallel Bus address = 1, card slot = 5.
2. Send the card select number and the command to interrogate positions B and C ("I" control block for listen operation):

   OUTPUT 709;"W1AA5"&"I1BC"

   The first portion of the output statement, "W1AA5", is a talk operation to select the card slot position of the module (A = 5). The second portion, "I1BC", is a listen operation which interrogates positions B and C of the selected card slot. The output statement can also be written as OUTPUT 709;"W1AA5I1BC".
3. Read back the information from the IEEE-488 bus and assign it to a string variable.

   ENTER 709;Result$

3.2.3 Programming Example

The following example shows how a programming word may be built using the IEEE-488 Bus Interface and HP 200 or 300 series computer. Please refer to the programing sheets.

In the Custom Termination Module a control word consists of:
"W$x S_1 S_2$abcdefghijklmnop"

"x" is the 4 Bit Parallel Bus address for the UTI-1 mainframe

"$S_1 S_2$" are the position selectors; ie. for positions A through J, S_1 = A an S_2 = J.

"a" is the card slot select address

"b through p" are control data values

Suppose the user had the following configuration requirements:

Connect Bus 1 to 600Ω in series with the tenth complex impedance.

1) The UTI-1 IEEE-488 bus address = 709, the 4 Bit Parallel Bus address = 1, and the card slot select address = 5.

   The output statement thus far is:

   OUTPUT 709;"W1AA5"

2) Connect Bus 1 to the intermediate bus.

   Intermediate Bus Tip connected to Bus #1 - B = 1

   Intermediate Bus Ring connected to Bus #1 - B = 2

   The output statement thus far is:

   OUTPUT 709;"W1AB53"

3) Connect programmable decadic resistance and the complex impedance to the intermediate bus. Connect the programmable decadic resistance in series with the complex impedance.

   Programmable decadic resistance connected to Intermediate Bus - C = 1

   Complex impedance connected to Intermediate Bus - C = 2

   Complex impedance connected in series with programmable decadic resistance-C = 4

   The output statement thus far is:

   OUTPUT 709;"W1AC537"

4) Enable complex impedance. D = 1

   The output statement thus far is:

   OUTPUT 709;"W1AD5371"

5) Enable tenth complex impedance and disable all other complex impedances.

   Enable tenth complex impedance - F = 4

   Disable all other complex impedances - E & G through J = 0

   The output statement thus far is:

   OUTPUT 709;"W1AJ5371040000"

6) Set programmable decadic resistance to 600Ω.

   Set decade 10^0 to 0Ω - K = 0
   Set decade 10^1 to 0Ω - L = 0
   Set decade 10^2 to 600Ω - M = 6
   Set decade 10^3 to 0Ω - N = 0
   Set decade 10^4 to 0Ω - O = 0
   Set decade 10^5 to 0Ω - P = 0

   The complete output statement is:

   OUTPUT 709;"W1AD5371040000006000"

3.3. Circuit Description

3.3.1 4 Bit Parallel Bus

The $\overline{\text{CARD SEL}}$ (card select) and $\overline{\text{TALK}}$/LISTEN input signals are combined in IC 4 and IC 5. The TALK/LISTEN input controls whether the low card select pulses are enabling the talk or listen circuitry. When in the talk mode, a low is at St2 pin 45A. This causes the enabling card select pulses to be at IC 4 pin 3. When in the listen mode, a high is at St2 pin 45A. This causes the enabling card select pulses to be at IC 4 pin 6.

Program positions A through P are accomplished by using the POS 2^3 input to switch between two sets of latches. When programming positions B through H, low pulses will be present at IC 4 pin 8, and when programming positions I through P, low pulses will be present at IC 4 pin 11. The pulses at IC 4 pin 8 will cause latches ICs 6 through 9 to be activated, and the pulses at IC 4 pin 11 will cause latches ICs 10 through 13 to be activated. ICs 6 and 10 latch the TALK 2^0 data, ICs 7 and 11 latch the TALK 2^1 data, ICs 8 and 12 latch the TALK 2^2 data,and ICs 9 and 13 latch the TALK 2^3 data. This latched data is connected to invertor driver ICs which activate the relays.

When in the listen mode, the low pulses at IC 4 pin 6 enables IC 3. Pin 14 of this IC pulses when interrogating position B, and pin 13 pulses when interrogating position C. These pulses enable IC 2. When interrogating position B pins 11, 13, 15, and 17 of IC 2 are latched to the listen ports, and when interrogating position C, pins 2, 4, 6, and 8 of IC 2 are latched to the listen ports. The computer will read this information back as a 0 in position B and a 6 in position C. This information corresponds to the card identification number 06.

3.3.2 Intermediate Bus and Wire Wrap Connections

Bus #1 and Bus #2 can be connected to any pair of Analog Bus pins from motherboard channels 1 through 6 or any pair of pins from the ten Bu 1 (Interchangeable Test Adapter connections) pins. Custom Termination Module Bus #1 is normally connected to motherboard Analog Bus 4, and Bus #2 is normally not connected.

The intermediate bus connects Bus #1 to the decadic resistance network and or the custom impedance section. When Relays 1, 2, and 5 are energized, Bus #1 is connected through the intermediate bus to the decadic resistance network. When Relays 1, 2, 6, and 9 are energized, Bus #1 is connected through the intermediate bus to the custom complex impedance section. When Relays 1, 2, 5, 6, and 9 are energized, Bus #1 is connected through the intermediate bus to the parallel combination of the custom complex impedance section and the decadic resistance network. When Relays 1, 2, 5, 7, and 9 are energized, Bus #1 is connected through the intermediated bus to the series combination of the custom complex impedance section and the decadic resistance network. When Relays 8 and 9 are energized, Bus #2 is connected to the custom complex impedance section.

3.3.3 Programmable Decadic Resistance

The programmable decadic resistance network consists of series resistors or resistor combinations which are each shorted out by relays in the non-energized position. Therefore with no relays energized, the impedance value of this network is 0 ohms. When each relay is energized, a resistor is placed in series. With each additional relay energized, another resistor is placed in series.

The resistors are grouped in steps of 1Ω, 10Ω, 100Ω, 1KΩ, 10KΩ, and 100KΩ steps. The 1Ω steps consist of 1Ω, 2Ω, 4Ω, and 8Ω resistors or resistor combinations. Different combinations of these resistors give 0Ω to 15Ω in 1Ω steps. The 10Ω steps consist of 10Ω, 20Ω, 40Ω, and 80Ω resistors or resistor combinations. Different combinations of these resistors give 0Ω to 150Ω in 10Ω steps. The 100Ω steps consist of 100Ω, 200Ω, 400Ω, and 800Ω resistors or resistor combinations. Different combinations of these resistors give 0Ω to 1500Ω in 100Ω steps. The 1KΩ steps consist of 1KΩ, 2KΩ, 4KΩ, and 8KΩ resistors or resistor combinations. Different combinations of these resistors give 0Ω to 15KΩ in 1KΩ steps. The 10KΩ steps consist of 10KΩ, 20KΩ, 40KΩ, and 80KΩ resistors or resistor combinations. Different combinations of these resistors give 0Ω to 150KΩ in 10KΩ steps. The 100KΩ steps consist of 100KΩ, 200KΩ, 400KΩ, and 800KΩ resistors or resistor combinations. Different combinations of these resistors give 0Ω to 1500KΩ in 100KΩ steps. Different combinations of all of the above mentioned resistors give 0Ω to 1.66525MΩ.

3.3.4 Custom Complex Impedances

The custom complex impedance section consists of 27 different relays which connect E points to the tip line of the circuit and F points to the ring line of the Circuit. There are two types of relay and pin configurations used. See the following figure.

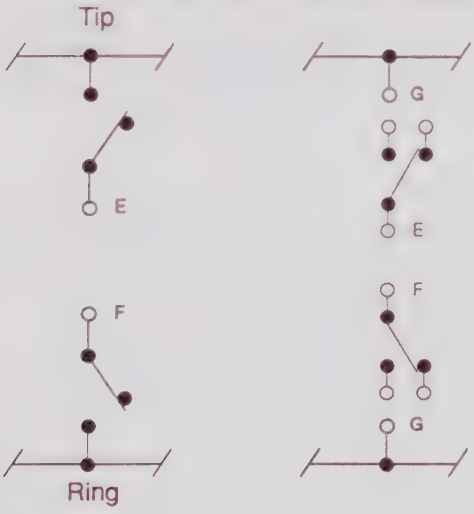
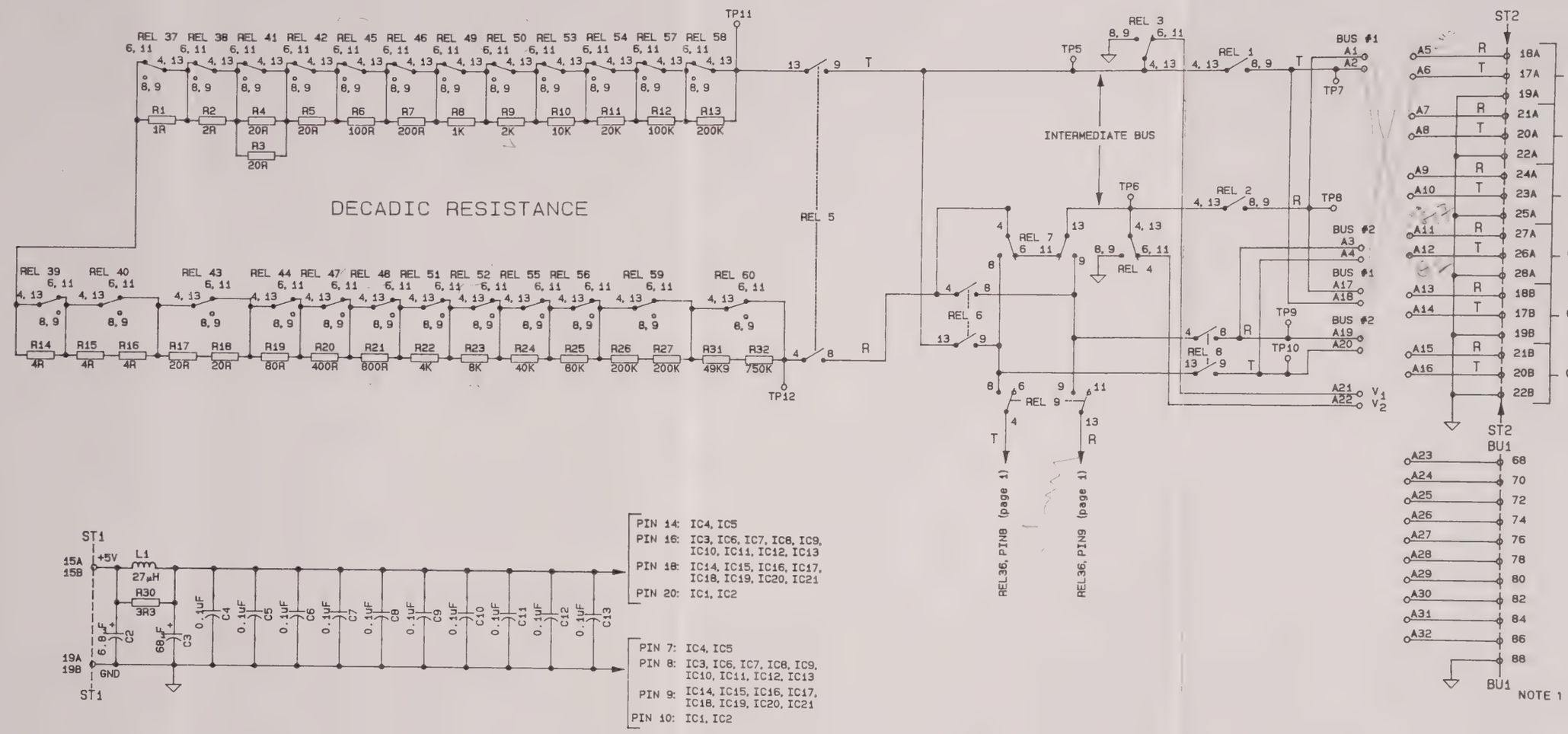


Figure 3.3.4 Relay and pin types for complex impedances.



NOTE:
1) FOR FUTURE USE, PINS 33 THRU 63 OF BU1 ARE NOT AVAILABLE IN THIS SERIES.

THIS DRAWING IS OUR PROPERTY. IT IS NOT TO BE COPIED OR USED WITHOUT THE WRITTEN CONSENT OF:

WANDEL & GOLTERMANN, INC.

	DATE	NAME	REV	ECN-NO	DATE	NAME
DRAWN	30-7-87	GARRETT	1	NEW	30-7-87	L M G
CHKD	6-1-88	HOOVER	2	87-211	5JAN88	M T S
APPRVD			3	88-061	21APR88	LMG
REPLACES						
REPLCD BY						

CUSTOM TERMINATION

SERIES A

9537-7506.XX/B

PG 1 OF 3

REV	ECN-NO	DATE	NAME
1	NEW	30-7-87	L M G
2	87-211	5JAN88	M T S
3	88-061	21APR88	L M G

	NAME	DATE
DRAWN	GARRETT	30-7-87
CHKD		21 April 88
APPRVD		
REPLACES		
REPLCD BY		

THIS DRAWING IS OUR PROPERTY.
IT IS NOT TO BE COPIED OR USED
WITHOUT THE WRITTEN CONSENT OF:
WANDEL & GOLTERMANN, INC.

COMPLEX IMPEDANCE

TP3 — R28 0R — TP1 — TIP

G1 G2 G3 G4 G5 G6 G13 G14 G15

REL 10 REL 11 REL 12 REL 13 REL 14 REL 15 REL 16 REL 17 REL 18 REL 19 REL 20 REL 21 REL 22 REL 23 REL 24 REL 25 REL 26 REL 27 REL 28 REL 29 REL 30 REL 31 REL 32 REL 33 REL 34 REL 35 REL 36

1E 2E 3E 4E 5E 6E 7E 8E 9E 10E 11E 12E 13E 14E 15E 16E 17E 18E 19E 20E 21E 22E 23E 24E 25E 26E 27E

330Ω (1/2W)

450Ω (1/2W)

3.4MF (100V)

1F 2F 3F 4F 5F 6F 7F 8F 9F 10F 11F 12F 13F 14F 15F 16F 17F 18F 19F 20F 21F 22F 23F 24F 25F 26F 27F

REL 10 REL 11 REL 12 REL 13 REL 14 REL 15 REL 16 REL 17 REL 18 REL 19 REL 20 REL 21 REL 22 REL 23 REL 24 REL 25 REL 26 REL 27 REL 28 REL 29 REL 30 REL 31 REL 32 REL 33 REL 34 REL 35 REL 36

G16 G17 G18

G7 G8 G9 G10 G11 G12

R29 0R

TP4 — TP2 — RING

→ REL9, PIN4 (page3)

→ REL9, PIN13 (page3)

FOR SERIES D... GROUND INFO:	FOR SERIES A THRU D; EXCEPT WITH MODIFICATION 254B: ADDITIONAL GNDS ARE:
ST1 GND POINTS: 19A, 24A, 26A, 32A, 38A, 40A, 42A, 44A, 46A, 48A 19B, 27B, 37B, 39B, 41B, 43B, 45B, 47B, 49B	ST1 GND POINTS: 19B, 20A, 22A, 28A, 30A, 34A, 36A, 50A, 21B, 23B, 25B, 29B, 31B, 33B, 35B,
ST2 GND POINTS: 8A, 14A, 9B, 15B	ST2 GND POINTS: 2A, 4A, 6A, 10A, 12A, 1B, 3B, 5B, 7B, 11B, 13B

GB

CUSTOM TERMINATION

SERIES A...

9537-7506.XX/B

PG 2 OF 3

POSITION

TALK DATA

50A 49A 48A 47A 44A 43A 42A 41A

ST2

IC 1 HC 244

45A TALK/LISTEN

IC 3 62B 62A HC 138

IC 2 HC 244

BOARD I.D. = 06

50B CARD SEC

ST2

LISTEN DATA 2^3 LISTEN DATA 2^2 LISTEN DATA 2^1 LISTEN DATA 2^0 RESET

41B 42B 43B 44B 49B

HC32 IC 4

HC86 IC 5

+5V

ULN 2803 IC 14 IC 15 IC 16 IC 17 IC 18 IC 19 IC 20 IC 21

HC 259 IC 6 IC 7 IC 8 IC 9 IC 10 IC 11 IC 12 IC 13

REL 1 REL 2 REL 3 REL 4 REL 5 REL 6 REL 7 REL 8 REL 9 REL 10 REL 11 REL 12 REL 13 REL 14 REL 15 REL 16 REL 17 REL 18 REL 19 REL 20 REL 21 REL 22 REL 23 REL 24 REL 25 REL 26 REL 27 REL 28 REL 29 REL 30 REL 31 REL 32 REL 33 REL 34 REL 35 REL 36 REL 37 REL 38 REL 39 REL 40 REL 41 REL 42 REL 43 REL 44 REL 45 REL 46 REL 47 REL 48 REL 49 REL 50 REL 51 REL 52 REL 53 REL 54 REL 55 REL 56 REL 57 REL 58 REL 59 REL 60

2^0 DATA 2^1 DATA 2^2 DATA 2^3 DATA

THIS DRAWING IS OUR PROPERTY.
IT IS NOT TO BE COPIED OR USED
WITHOUT THE WRITTEN CONSENT OF:
WANDEL & GOLTERMANN, INC.

REV	ECN-NO	DATE	NAME
1	NEW	30-7-87	L M G
2	87-211	5JAN88	M T S
3	88-041	11APR88	L.M.G.

	DATE	NAME
DRAWN	30-7-87	GARRETT
CHKD	6-1-88	HOOVER
APPRVD		
REPLACES		
REPLCD BY		

CUSTOM TERMINATION

SERIES A

9537-7506.XX/B

PG 3 OF 3

3 10.11.12 22 13 1 13 16 14 20 4 20

13 15 7,8,9 17 22 6,8,9

PROTOTYPE AREA PROTOTYPE AREA

SEE DETAIL 'A' 21 5 13

DETAIL 'A'

PINS 33 TO 63 ARE FOR FUTURE USE AND ARE NOT AVAILABLE IN THIS SERIES ACTUAL BU1 CONNECTOR IS MARKED PINS 1 THRU 64. DETAIL DWG SHOWS PROPER PIN #'S AND LOCATION.

NOTE:
1. ALL AREAS WITHIN DOTTED LINES ARE TO BE SOLDERMASKED USING ITEM 18 OR ITEM 19

Ausgabe	Änderung	Tag	Name
4	88-059	13.4.88	LMG
3	ECN 87-163	18.11.87	DHP
2	ECN 87-035	28.5.87	
1	neu	25.9.91	W.S.

Oberfläche

Freimaßtoleranzen. WN 51/3/1

	Tag	Name
Bearb	23.3.87	Les Garrett
Gepr.	26.3.87	Sanjay
Norm.		

Wandel u. Goltermann Reutlingen

Halbzeug und Werkstoffe

Benennung: CUSTOM TERMINATION BD. (ASSEMBLED)

Maßstab: 1/1

9537-7006.00 /34

Ersatz für: Ersatz. Verwdg

WANDEL & GOLTERMANN TECHNOLOGIES, INC.

CUSTOM TERMINATION MODULE

BN 9537 ********** LIST OF REPLACEABLE PARTS ********** SERIES: ALL

DATE: Jan 8, 1990

DIAG	REF	ITEM	QTY	PART NUMBER	DESCRIPTION	STOCK LOCATION	VERS/OPT	SERIES STRT	SERIES END	SUBASSEMBLY 9537-XXXX	SUBASSEMBLY CODE
							00 06			7006	S
		0	0	9537-7006.001	CUSTOM TERMINATION		00 06			7006	A
		1	1	9537-7006.027	PC BOARD MACHINED		00 06			7006	
		3	1	9537-7006.056	PANEL REAR MARKED		00 06			7006	M
		5	1	0000-2911.029	LABEL SERIAL ABC		00 06			7006	
		6	1	9537-7001.064	BLOCK PANEL MTG 1		00 06			7006	
		7	2	9537-7001.080	BLOCK PANEL MTG 2		00 06			7006	
		12	32		RECEPT PIN ANG ROW#3	XX03-0518.00	00 06			7006	
		15	12	0000-2901.026	TERM SOLD WN34/5/8		00 06			7006	
		20	1	0001-0072.468	LABEL YEL/BLK C-MOS		00 06			7006	
		21	.1		TUBNG SHRNK 1/4" BLK	XX31-0005.00	00 06			7006	
		22	1		HEADR STR AU M1X36P	XX03-0375.00	00 06			7006	M
01	BU	1	1	9537-0000.101	CONN MODIFIED 64P		00 06			7006	M
06	C	2	1		C-ELYT TA 6.8U10%35V	XX32-0086.00	00 06			7006	
06	C	3	1		CAP TANT 68uF 6V	XX32-0085.00	00 06			7006	
06	C	4	1	0000-7632.659	C-CER 100N 10% 50V		00 06			7006	
06	C	5	1	0000-7632.659	C-CER 100N 10% 50V		00 06			7006	
06	C	6	1	0000-7632.659	C-CER 100N 10% 50V		00 06			7006	
06	C	7	1	0000-7632.659	C-CER 100N 10% 50V		00 06			7006	
06	C	8	1	0000-7632.659	C-CER 100N 10% 50V		00 06			7006	
06	C	9	1	0000-7632.659	C-CER 100N 10% 50V		00 06			7006	
06	C	10	1	0000-7632.659	C-CER 100N 10% 50V		00 06			7006	
06	C	11	1	0000-7632.659	C-CER 100N 10% 50V		00 06			7006	
06	IC	1	1	0000-7594.959	IC MOS 74HC244 D20		00 06			7006	
06	IC	2	1	0000-7594.959	IC MOS 74HC244 D20		00 06			7006	
06	IC	3	1	0000-7597.309	IC MOS 74HC138 D16		00 06			7006	
06	IC	4	1	0000-7597.176	IC MOS 74HC32 D14		00 06			7006	
06	IC	5	1	0000-7597.244	IC MOS 74HC86 D14		00 06			7006	
06	IC	6	1	0000-7597.590	IC MOS 74HC259 D16		00 06			7006	
06	IC	7	1	0000-7597.590	IC MOS 74HC259 D16		00 06			7006	
06	IC	8	1	0000-7597.590	IC MOS 74HC259 D16		00 06			7006	
06	IC	9	1	0000-7597.590	IC MOS 74HC259 D16		00 06			7006	
06	IC	10	1	0000-7597.590	IC MOS 74HC259 D16		00 06			7006	
06	IC	11	1	0000-7597.590	IC MOS 74HC259 D16		00 06			7006	
06	IC	12	1	0000-7597.590	IC MOS 74HC259 D16		00 06			7006	
06	IC	13	1	0000-7597.590	IC MOS 74HC259 D16		00 06			7006	

WANDEL & GOLTERMANN TECHNOLOGIES, INC.

CUSTOM TERMINATION MODULE

DN 9537 ********** LIST OF REPLACEABLE PARTS ********** SERIES: ALL

DATE: Jan 8, 1990

DIAG	REF	ITEM	QTY	PART NUMBER	DESCRIPTION	STOCK LOCATION	VERS/OPT	SERIES STRT	SERIES END	SUBASSEMBLY 9537-XXXX CODE
06	IC	14	1	0000-7579.657	IC DRVR ULN2803A D18		00 06			7006
06	IC	15	1	0000-7579.657	IC DRVR ULN2803A D18		00 06			7006
06	IC	16	1	0000-7579.657	IC DRVR ULN2803A D18		00 06			7006
06	IC	17	1	0000-7579.657	IC DRVR ULN2803A D18		00 06			7006
06	IC	18	1	0000-7579.657	IC DRVR ULN2803A D18		00 06			7006
06	IC	19	1	0000-7579.657	IC DRVR ULN2803A D18		00 06			7006
06	IC	20	1	0000-7579.657	IC DRVR ULN2803A D18		00 06			7006
06	IC	21	1	0000-7579.657	IC DRVR ULN2803A D18		00 06			7006
06	L	1	1	0001-0042.757	L-FERRITE 27U HORIZ		00 06			7006
06	R	1	1		R-WW 1R 1% 3W TC50	XX08-0784.00	00 06			7006
06	R	2	1		R-WW 2R 1% 3W TC50	XX08-0785.00	00 06			7006
06	R	3	1		R-WW 20R 1% 3W TC20	XX08-0788.00	00 06			7006
06	R	4	1		R-WW 20R 1% 3W TC20	XX08-0788.00	00 06			7006
06	R	5	1		R-WW 20R 1% 3W TC20	XX08-0788.00	00 06			7006
06	R	6	1		R-MF 100R 1% 2W TC50	XX08-0790.00	00 06			7006
06	R	7	1		R-MF 200R 1% 2W TC50	XX08-0791.00	00 06			7006
06	R	8	1		R-MF 1K 1% 2W TC50	XX08-0794.00	00 06			7006
06	R	9	1		R-MF 2K 1% 2W TC50	XX08-0795.00	00 06			7006
06	R	10	1		R-MF 10K 1% 2W TC50	XX08-0801.00	00 06			7006
06	R	11	1		R-MF 20K 1% 2W TC50	XX08-0804.00	00 06			7006
06	R	12	1	0000-7519.536	R-MF 100K 1% 204		00 06			7006
06	R	13	1	0000-7633.991	R-MF 200K 1% 204		00 06			7006
06	R	14	1		R-WW 4R 1% 3W TC50	XX08-0786.00	00 06			7006
06	R	15	1		R-WW 4R 1% 3W TC50	XX08-0786.00	00 06			7006
06	R	16	1		R-WW 4R 1% 3W TC50	XX08-0786.00	00 06			7006
06	R	17	1		R-WW 20R 1% 3W TC20	XX08-0788.00	00 06			7006
06	R	18	1		R-WW 20R 1% 3W TC20	XX08-0788.00	00 06			7006
06	R	19	1		R-MF 80R 1% 2W TC50	XX08-0789.00	00 06			7006
06	R	20	1		R-MF 400R 1% 2W TC50	XX08-0792.00	00 06			7006
06	R	21	1		R-MF 800R 1% 2W TC50	XX08-0793.00	00 06			7006
06	R	22	1		R-MF 4K 1% 2W TC50	XX08-0797.00	00 06			7006
06	R	23	1		R-MF 8K 1% 2W TC50	XX08-0798.00	00 06			7006
06	R	24	1		R-MF 40K 1% 2W TC50	XX08-0805.00	00 06			7006
06	R	25	1		R-MF 80K 1% 2W TC50	XX08-0806.00	00 06			7006
06	R	26	1	0000 7633.991	R-MF 200K 1% 204		00 06			7006
06	R	27	1	0000-7633.991	R-MF 200K 1% 204		00 06			7006

WANDEL & GOLTERMANN TECHNOLOGIES, INC.

CUSTOM TERMINATION MODULE

BN 9537 ********** LIST OF REPLACEABLE PARTS ********** SERIES: ALL DATE: Jan 8, 1990

DIAG	REF	ITEM	QTY	PART NUMBER	DESCRIPTION	STOCK LOCATION	VERS/OPT	SERIES STRT	SERIES END	SUBASSEMBLY 9537-XXXX CODE
06	R	28	1	0000-7555.228	R-MF 0 OHM JUMP 207		00 06			7006
06	R	29	1	0000-7555.228	R-MF 0 OHM JUMP 207		00 06			7006
06	R	30	1	0000-7629.743	R-MF 3.32R 2% 204		00 06			7006
06	R	31	1	0000-7618.343	R-MF 49.9K 1% 204		00 06			7006
06	R	32	1		R-MF 750K .1% 1/4W	XX08-0630.00	00 06			7006
06	REL	1	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 06			7006
06	REL	2	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 06			7006
06	REL	3	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 06			7006
06	REL	4	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 06			7006
06	REL	5	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 06			7006
06	REL	6	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 06			7006
06	REL	7	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 06			7006
06	REL	8	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 06			7006
06	REL	9	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 06			7006
06	REL	10	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 06			7006
06	REL	11	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 06			7006
06	REL	12	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 06			7006
06	REL	13	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 06			7006
06	REL	14	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 06			7006
06	REL	15	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 06			7006
06	REL	16	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 06			7006
06	REL	17	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 06			7006
06	REL	18	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 06			7006
06	REL	19	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 06			7006
06	REL	20	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 06			7006
06	REL	21	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 06			7006
06	REL	22	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 06			7006
06	REL	23	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 06			7006
06	REL	24	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 06			7006
06	REL	25	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 06			7006
06	REL	26	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 06			7006
06	REL	27	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 06			7006
06	REL	28	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 06			7006
06	REL	29	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 06			7006
06	REL	30	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 06			7006
06	REL	31	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 06			7006

WANDEL & GOLTERMANN TECHNOLOGIES, INC.
CUSTOM TERMINATION MODULE

BN 9537 ********** LIST OF REPLACEABLE PARTS ********** SERIES: ALL
DATE: Jan 8, 1990

DIAG	REF	ITEM	QTY	PART NUMBER	DESCRIPTION	STOCK LOCATION	VERS/OPT	SERIES STRT	SERIES END	SUBASSEMBLY 9537-XXXX	SUBASSEMBLY CODE
06	REL	32	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 06				7006
06	REL	33	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 06				7006
06	REL	34	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 06				7006
06	REL	35	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 06				7006
06	REL	36	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 06				7006
06	REL	37	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 06				7006
06	REL	38	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 06				7006
06	REL	39	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 06				7006
06	REL	40	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 06				7006
06	REL	41	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 06				7006
06	REL	42	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 06				7006
06	REL	43	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 06				7006
06	REL	44	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 06				7006
06	REL	45	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 06				7006
06	REL	46	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 06				7006
06	REL	47	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 06				7006
06	REL	48	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 06				7006
06	REL	49	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 06				7006
06	REL	50	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 06				7006
06	REL	51	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 06				7006
06	REL	52	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 06				7006
06	REL	53	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 06				7006
06	REL	54	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 06				7006
06	REL	55	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 06				7006
06	REL	56	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 06				7006
06	REL	57	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 06				7006
06	REL	58	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 06				7006
06	REL	59	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 06				7006
06	REL	60	1		RELAY DS-2ES-DC5V	XX07-0042.00	00 06				7006

Wandel & Goltermann

Electronic Measurement Technology